

# Service Manual

Personal Computer  
**JR-200U**

## Specifications

CPU:	MN1800A (equivalent to 6802)
Memory:	16K ROM (BASIC) 32K RAM 2K Video RAM 2K Character RAM
Keyboard:	
Mode:	Sub CPU Transfer
Key:	63 Keys
Display Interface:	
Mode:	RGB Sync Separation Composite Video System RF Modulation (Ch-3 and 4)
Screen:	24 Lines by 32 Columns
Color:	8 Colors
Graphic:	64 by 48 Dot Matrix
Character Configuration:	
Alphanumeric:	95 Characters
Graphic Symbols:	64 Characters
Other Symbols:	17 Characters
User's Definition:	64 Characters
Music:	A compass of 5 octaves allows performance of melody consisting triad cords
Cassette Interface:	600/2400 BAUD Rate Changeable
Printer Interface:	Centronics Standard
Joystick Interface:	Two Sockets
Program Language:	JR-BASIC5.0 and Machine Language
Constants:	
Decimal:	$10^{-39}$ to $10^{-38}$ and 0
Hexadecimal:	\$0 to \$FFFF
Power Source:	AC 120 V $\pm$ 10%, 50/60 Hz
Power Consumption:	8 W max.
Dimensions:	W: 2-3/16" (56 mm) D: 13-7/10" (348 mm) H: 8-1/5" (208 mm) Approx. 5-1/16 lbs. (2-3 kg)
Weight:	
Accessory:	RF Cables, Recording Cable and Antenna Selector



## General Instructions

- Refer to the Operating Instruction for operation and BASIC language.
- To check the performance, please use the Diagnostic Program.
- Do not use thinner, benzine or alcohol to clean the cabinet.
- Use a silicone treated cloth or a cloth dampened with a gentle cleaning liquid that will not damage the cabinet.

Specifications are subject to change without notice.

# Panasonic®

Matsushita Engineering and Service Company  
Division of Matsushita Electric Corporation of America  
50 Meadowland Parkway,  
Secaucus, New Jersey 07094

Panasonic Hawaii, Inc.  
91-238 Kauhi St. Ewa Beach.  
P.O.Box 774  
Honolulu, Hawaii 96808-0774

Matsushita Electric of Canada Limited  
5700 Ambler Drive, Mississauga,  
Ontario, L4W 2T3

Panasonic Sales Company,  
Division of Matsushita Electric of Puerto Rico, Inc.  
Ave., 65 De Infanteria, KM 9.7  
Victoria Industrial Park  
Carolina, Puerto Rico 00630

Panasonic Tokyo  
Matsushita Electric Industrial Co., Ltd.  
1-2, 1-chome, Shibakoen, Minato-ku,  
Tokyo 105, Japan

# Table of Contents

	Page
1. Diagnostic Programs	1
1.1. RAM Test Program	1
1.2. ROM Test Program	1
1.3. Function Check Program	2
2. Block Diagram	17
3. Signal Code Table	18
3.1. Address Bus Signals	18
3.2. Data Bus Signals	18
3.3. Sub CPU	18
3.4. External Bus	19
3.5. Printer Interface	19
4. Memory Map	20
5. Schematic Diagram	21
5.1. Power Supply and Keyboard	21
5.2. Main P.C.B.	23
6. Parts Location	24
6.1. Main P.C.B.	24
6.2. Keyboard	25
6.3. Power Supply	25
7. Waveforms	26
7.1. Power-on Reset Timing	26
7.2. Basic Timing	26
7.3. Dynamic RAM R/W Timing	26
7.4. CRTC Basic Timing	27
7.5. CRTC Synchronizing Timing	28
7.6. Keyboard Scanning	28
8. Circuit Descriptions	29
8.1. Basic Timing Generator	29
8.2. CPU	29
8.3. Dynamic RAM	33
8.4. ROM	35
8.5. Video Refresh RAM	37
8.6. Character Generator RAM	38
8.7. CRT Controller and Video Interface	39
8.8. I/O Interface (PIA)	51
8.9. Interrupt Control	58
9. Character Code	60
9.1. Display Code Table (Hexadecimal Value)	60
9.2. Character (ASCII) Code Table (Hexadecimal Value)	60
10. Connector Pin Identification	61
10.1. Display Connector	61
10.2. Tape Recorder Connector	61
10.3. Printer Connector	61
10.4. Joystick Connector	62
10.5. External Bus Connector	62
10.6. RS-232C Connector (Optional)	63
11. LSI & IC Pin Configuration	64
11.1. MN1800A CPU	64
11.2. MN1544CJR Sub CPU	65
11.3. MN4864CA2 (ROM 0), MN4864CB2 (ROM 1)	66
11.4. HM4864P3 RAM	66
11.5. HM6116P3 RAM	67
11.6. MN1271 PIA	67
11.7. CRTC HD61K201F	69
11.8. TTL ICs	71
12. Disassembly	73
13. Exploded View	74
14. Troubleshooting	75
15. Packing	79
16. Replacement Parts List	80

## 1. Diagnostic Programs

The JR-200U diagnostic program consists of three programs for use in RAM, ROM, and the Function Checking.

### 1.1. RAM Test Program (See the program list -1.)

This program is used to detect malfunctions in the JR-200U dynamic RAM, Video RAM, and character RAM.

When a malfunction is detected an error message is displayed on the screen and processing is halted.

The RAM test program is written entirely in machine language, and can be executed only once because it will rewrite data of all RAMs. Turn the main switch off and on when you want to load another program into the JR-200U.

#### (1) Operation Procedure

- a. Switch the power supply ON.
- b. Use the MLOAD command to load the program from cassette.
- c. Input F=USR (\$1100) from the keyboard to run the program.
- d. The following message will appear on the screen when the RAM test is completed normally.  
RAM-TEST NORMAL END  
Ready

If a malfunction is detected, an error message indicating the number of the malfunctioning IC will be displayed on the screen and processing will be halted.

- i) One of the following messages will appear on the screen when a dynamic RAM malfunctions.  
D-RAM ERROR!  
DEVICE = IC8  
Ready  
or  
D-RAM ERROR!  
DEVICE = IC9  
Ready  
or  
D-RAM ERROR!  
DEVICE = IC10  
Ready  
or  
D-RAM ERROR!  
DEVICE = IC11  
Ready
- ii) Video RAM malfunction  
V-RAM ERROR!  
DEVICE = IC7  
Ready
- iii) Character RAM malfunction  
C-RAM ERROR!  
DEVICE = IC6  
Ready

### 1.2. ROM Test Program (See the program list -2.)

This program is used to detect malfunctions in the two ROMs used in the JR-200U.

When a malfunction is detected an error message is displayed on the screen and processing is halted.

The ROM test program is written entirely in machine language.

#### (1) Operation Procedure

- a. Switch the power supply ON.
- b. Use the MLOAD command to load the program from cassette.
- c. Input F=USR (\$1000) from the keyboard to run the program.
- d. The following message will appear on the screen when the ROM test is completed normally.  
ROM-TEST NORMAL END  
Ready

If a malfunction is detected, an error message indicating the number of the malfunctioning IC will be displayed on the screen and processing will be halted.

One of the following messages will appear on the screen if a ROM malfunctions.

ROM ERROR!

DEVICE = IC4

Ready

or

ROM ERROR!

DEVICE = IC5

Ready

### 1.3. Function Check Program (See the program lists 3 and 4.)

This program is used to check Functions of the JR-200U. It tests the following items.

- \* Printer output
- \* CRT color balance
- \* CRT distortion
- \* Semi-graphic output
- \* User defined pattern output
- \* Keyboard input
- \* Joystick input
- \* Speaker output
- \* Cassette tape MSAVE, MLOAD and VERIFY

This program consists of both BASIC and machine language programs.

#### (1) Operation Procedure

- a. Switch the power supply ON.
- b. Use the LOAD command to load the program from cassette.
- c. Use the MLOAD command to load the machine language program from cassette.
- d. Run the program with the RUN command.
- e. Printer output test

Check that the following data is printed normally.

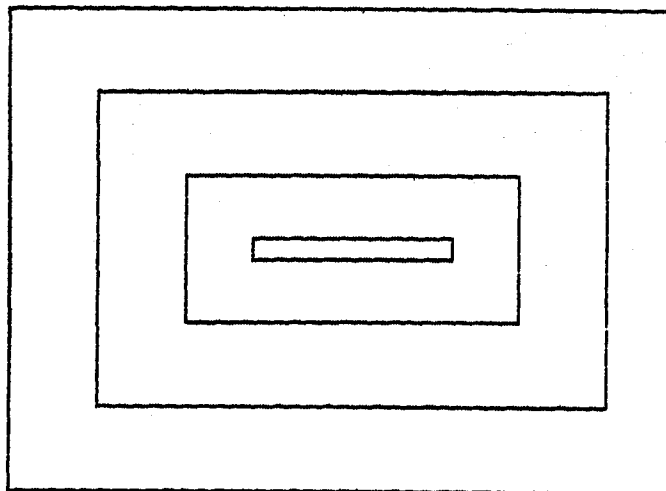
1234567890abcdefghijklmnopqrstuvwxyz!"#\$%&'(<=>~|`(+\*<>?\_@CJ:;.,  
/ABCDEFGHIJKLMNPOQRSTUVWXYZ

- f. CRT color balance test
  - i) Check that the color of the color bars appearing on the screen.

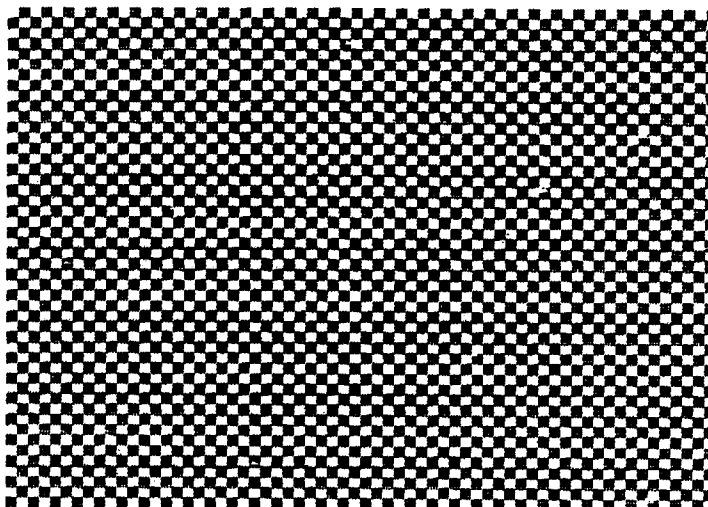
Black	Blue	Red	Magenta	Green	Cyan	Yellow	White

- ii) Press any key to proceed to the next test.
- g. CRT distortion test
  - i) Check that the pattern appearing on the screen is not distorted.

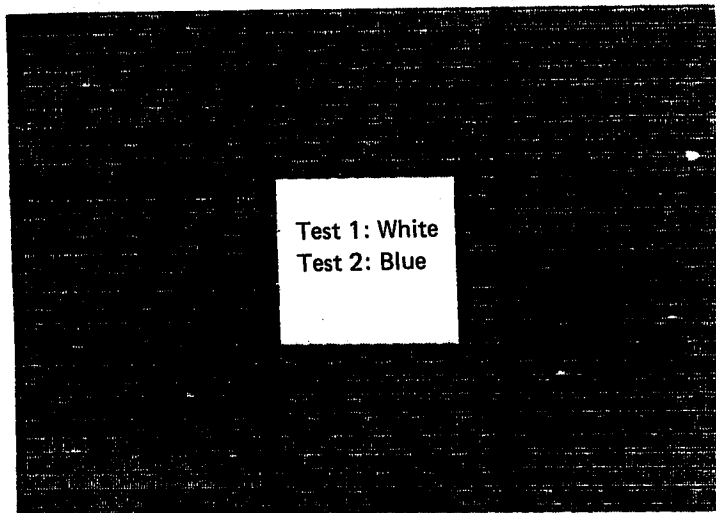




- ii) Press any key to proceed to the next test.
- h. Semi-graphic output test
  - i) Check that the semi-graphic pattern appearing on the screen is normal.



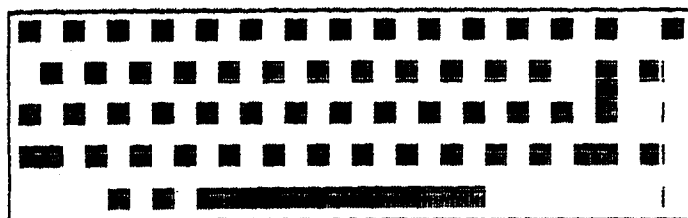
- ii) Press any key to proceed to the next test.
- i. User defined pattern test
  - i) Check that the user defined pattern appearing on the screen is normal.
  - ii) Test 1
    - Characters = White
    - Background = Blue
  - iii) Press any key to proceed to the next test.
  - iv) Test 2
    - Characters = Blue
    - Background = White



Test 1: Blue  
Test 2: White

- v) Press any key to proceed to the next test.
- j. Keyboard input test

#### KEYBOARD TEST



HIT BLINKING KEY  
HIT 1 KEY

- i) Press the keys indicated on the screen.
- ii) Press the SHIFT key as indicated on the screen.
- iii) Press the 

GRAPH
ON

 and 

GRAPH
OFF

 keys as indicated on the screen.
- iii-i) Press the 

GRAPH
ON

 key, and then press "X" key.
- iii-ii) Press the 

GRAPH
ON

 key, and then press "Z" key.
- iv) Press the CTRL+C key as indicated on the screen.

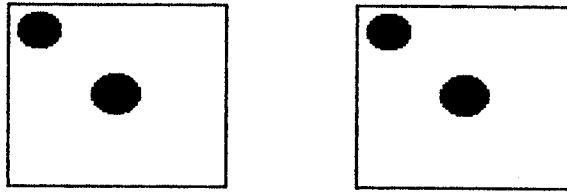
HIT CTRL+C, AND THEN HIT RETURN  
KEY

GOTO 690

After pressing CTRL+C to halt processing, return to the program by inputting GOTO 690 from the keyboard.

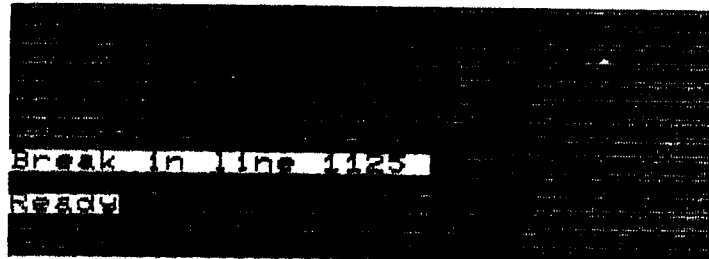
k. Joystick input test

JOYSTICK TEST 1



MOVE THE JOYSTIC LEVER IN  
THE DIRECTION OF THE ARROW.

- i) Move joystick 1 as indicated on the screen.
  - ii) Press the joystick switch as indicated on the screen.
  - iii) Move joystick 2 as indicated on the screen.
  - iv) Press the joystick switch as indicated on the screen.
- l. Speaker output test
- i) The same pattern as with the color balance test will appear on the screen and music will be played from the speaker in monotones (tones are emitted by three sound sources in succession). If the music is played normally, press the BREAK key to return to the program.



- m. Use the CLS command (CTRL+1) to clear the screen.
- n. Cassette tape test
  - i) Input GOTO 1400 to start the program again.
  - ii) Connect the cassette tape recorder and press the record button.
  - iii) Press the RETURN key. (Saving)

```
          CASSETTE TEST
READY
MSAVE "CASSETTETEST", $1000, $137F
PUSH record
PUSH CASSETTETEST
VERIFY
PUSH play
PUSH CASSETTETEST
READY
```

HIT RETURN KEY

- iv) Rewind the cassette, press the play button, and then press the RETURN key. (Verifying)
- v) Confirm that "Ready" message appears on the screen without any error message.

(2) Processing at Error

If an error occurs during program execution, the program will stop at the step at which the error occurred (only with keyboard and joystick input tests).



## JR-200 MEMORY DUMP V1.0

**PAGE : 1**

[illegible]

## CHARACTERS

[illegible]

## CHARACTERS

[illegible]

## JR-200 MEMORY DUMP V1.0

PAGE : 2

[illegible]

## CHARACTERS

[illegible]

## CHARACTERS

[illegible]

PAGE 11

JR-200 TEST PROGRAM      I/O TEST BASIC PROGRAM

```

1 REM *****
2 REM ** JR-200 TEST PRO. **
4 REM ** 1982/12/9 **
5 REM ** H.YASUI **
6 REM *****
10 REM ** MAIN **
20 CLS:GOSUB 1300:GOSUB 700:GOSUB 800:GOSUB 900:GOSUB 1000:GOTO 100
30 GOSUB 3200:GOSUB 1100
40 END
100 REM ** KEY IN TEST **
110 B=USR($A08,$A400):COLOR 7,0,0:CLS:LOCATE 10,3:PRINT "KEYBOARD TEST"
120 FOR I=1 TO 400:NEXT
130 PRINT " ";
140 PRINT " ";
150 PRINT " ";
160 PRINT " ";
170 PRINT " ";
180 PRINT " ";
190 PRINT " ";
200 PRINT " ";
210 PRINT " ";
220 PRINT " ";
230 PRINT " ";
240 COLOR 0,7:LOCATE 30,7:PRINT "I";LOCATE 30,9:PRINT "I"
250 LOCATE 30,11:PRINT "I";LOCATE 30,13:PRINT "I"
260 COLOR 7,0:LOCATE 4,19:PRINT "HIT BLINKING KEY"
270 LOCATE 4,21:I=$A468
280 D=PEEK(I):X=PEEK(I+1):Y=PEEK(I+2):S1=PEEK(I+3):S2=PEEK(I+4)
290 L1=PEEK(I+5):I=I+6:N=PEEK(I):K=CHR$(N):IF L1=1 THEN 310
300 FOR J=1 TO L1-1:N=PEEK(I+J):K=K+CHR$(N):NEXT

```

## CHARACTERS

[illegible]

## CHARACTERS

[illegible]

```

4400 IF S3=3 THEN S8="..." ;GOTO 450
4410 IF S3=4 THEN S8="X";GOTO 470
4420 IF S3=5 THEN S8=" " ;GOTO 470
4430 IF S3=6 THEN S8="Z";GOTO 470
4440 COLOR 0,7,0,PRINT M$;COLOR 7,0,PRINT " KEY";GOTO 490
4450 COLOR 0,7,0,PRINT M$;COLOR 7,0,PRINT " " + "I";COLOR 0,7,0,PRINT " "
4460 COLOR 7,0,0,PRINT M$;COLOR 7,0,PRINT " KEY";GOTO 490
4470 COLOR 0,7,0,PRINT M$;COLOR 7,0,PRINT " KEY"
4480 LOCATE 3,22,PRINT " ", AND THEN HIT "I";COLOR 0,7
4485 PRINT S$;COLOR 7,0,0,PRINT " KEY"
4490 C=0
4500 LOCATE X,Y;IF C=11 THEN COLOR 2,0,S1,PRINT K$;C=C+1;COLOR
4510 IF C<>6 THEN 550
4520 IF K$="I" THEN COLOR 2,0,0,PRINT " " ;GOTO 550
4530 IF K$=" " THEN COLOR 2,0,0,PRINT " " ;GOTO 550
4540 COLOR 2,0,2,PRINT K$
4550 C=C+1;PICK A;IF A=0 THEN 500
4570 IF D<>A THEN 500
4580 LOCATE X,Y;COLOR 7,1,S2,PRINT D$
4590 PICK W;IF W<>X THEN 620
4630 IF I<=475A THEN 280

```

```

4200 PICK W:IF W<>0 THEN 620
430 I=1<#4761 THEN 280
435 COLOR 7,0,0
440 CLS:LOCATE 0,2:COLOR 7,0,0:PRINT "HIT ";:COLOR 0,7:PRINT "CTRL+C";
450 COLOR 7,0:PRINT " ",AND THEN HIT "
460 COLOR 0,7:PRINT "RETURN";:COLOR 7,0:PRINT " KEY"
470 LOCATE 0,9:PRINT "GOTO 690"
480 LOCATE 0,5:GOTO 680
490 GOTO 30
700 REM ** COLOR TEST **
710 CLS:LOCATE 9,3:PRINT "COLOR TEST";FOR I=1 TO 400:NEXT
720 POKE #CA00,1:F=USR(#61F3)
730 PICK K:IF K=0 THEN 730
740 PICK K:IF K<>0 THEN 740
750 POKE #CA00,0:RETURN
800 REM ** LINE TEST **
810 CLS:LOCATE 10,3:PRINT "LINE TEST";FOR I=1 TO 400:NEXT:CLS
820 F=USR(#6270)
830 PICK K:IF K=0 THEN 830
840 PICK K:IF K<>0 THEN 840
850 RETURN
900 REM ** SEMIGRAPHICS TEST **
910 CLS:LOCATE 7,3:PRINT "SEMIGRAPHICS TEST";FOR I=1 TO 400:NEXT
920 F=USR(#6327)
930 PICK K:IF K=0 THEN 930
940 PICK K:IF K<>0 THEN 940
950 RETURN
1000 REM ** USER PATTERN TEST **
1010 CLS:LOCATE 9,3:PRINT "USER PATTERN TEST";FOR I=1 TO 400:NEXT
1020 F=USR(#6348,0,#FF)
1030 PICK K:IF K=0 THEN 1030
1040 PICK K:IF K<>0 THEN 1040
1050 F=USR(#6348,0,#0)
1060 PICK K:IF K=0 THEN 1060
1070 PICK K:IF K<>0 THEN 1070
1080 RETURN
1100 REM ** COLOR & SPEAKER TEST **
1105 G=USR(#61F3)
1110 TEMPO 50:PLAY "B",#5000,#5300,#5600:POKE #CA00,1
1120 IF PEEK($30)=0 THEN PLAY "B",#5000,#5300,#5600
1125 GOTO 1120
1130 PICK A:IF A=0 THEN 1120
1140 PICK E:IF E<>0 THEN 1140
1150 POKE #30,0:POKE #31,0:RETURN
1300 REM ** PRINTER TEST **
1310 CLS:LOCATE 10,3:PRINT "PRINTER TEST"
1320 LPRINT "1234567890abcdefghijklmnopqrstuvwxyz";
1340 LPRINT "1234567890abcdefghijklmnopqrstuvwxyz";
1350 LPRINT "ABCDEFGHIJKLMNOPQRSTUVWXYZ";RETURN
1400 REM ** CASSETTE TEST **
1410 POKE #CA00,0:COLOR 7,0,0:CLS:LOCATE 8,3:PRINT "CASSETTE TEST";POKE #2B,0
1430 LOCATE 0,5:PRINT "SAVE 'CASSETTETEST',#1000,#137F";
1440 LOCATE 0,10:PRINT "VERIFY ";LOCATE 7,20:COLOR 7,0:PRINT "HIT ";
1460 COLOR 0,7:PRINT "RETURN";:COLOR 7,0:PRINT " KEY";LOCATE 0,3:END
3200 REM ** JOYSTICK TEST **
3210 F=0:IF 2:COLOR 7,0,0:Z=USR(#6408,#4782)
3220 A#=CHR#($21)+CHR#($23)+CHR#($1D)+CHR#($1F)+CHR#($22)+CHR#($24)
3230 B#=CHR#($25)+CHR#($26)+CHR#($27)+CHR#($1D)+CHR#($1D)+CHR#($1D)
3240 B#=#B+CHR#($1F)+CHR#($2B)+CHR#($29)+CHR#($2A)+CHR#($1D)+CHR#($1D)
3250 B#=#B+CHR#($1D)+CHR#($1F)+CHR#($2B)+CHR#($2C)+CHR#($2D)
3260 C#=#B+CHR#($20)+CHR#($20)+CHR#($1D)+CHR#($1F)+CHR#($20)+CHR#($20)
3265 CLS
3260 C#=#CHR#($20)+CHR#($20)+CHR#($1D)+CHR#($1F)+CHR#($20)+CHR#($20)+CHR#($20)
3265 CLS
3270 LOCATE 8,0:PRINT "JOYSTICK TEST";F=1
3280 D#=#1
3290 LOCATE 2,2:PRINT " "
3300 LOCATE 2,3:PRINT D#;LOCATE 2,4:PRINT D#;LOCATE 2,5:PRINT D#
3310 LOCATE 2,6:PRINT D#;LOCATE 2,7:PRINT D#;LOCATE 2,8:PRINT D#
3320 LOCATE 2,9:PRINT D#;LOCATE 2,10:PRINT D#;LOCATE 2,11:PRINT D#
3380 LOCATE 2,12:PRINT " "
3390 COLOR 7,0,1:LOCATE 3,3:PRINT A#;LOCATE 6,6:PRINT B#
3395 LOCATE 19,3:PRINT A#;LOCATE 22,6:PRINT B#
3400 COLOR 7,0,0:LOCATE 3,17:PRINT "MOVE THE JOYSTICK LEVER IN "
3410 LOCATE 2,18:PRINT "THE DIRECTION OF THE ARROW.";I=#4818
3420 P=PEEK(1):256+PEEK(1+1):K=PEEK(1+2):L=PEEK(1+3):D=PEEK(1+4)
3430 A=P+8400:IF F=1 THEN P=P+16:A=A+16
3440 N=7:D=0
3460 IF C=11 THEN POKE A,2:POKE P,K:K=C=0:GOTO 3480
3470 IF C=6 THEN POKE A,2:POKE P,#20
3480 C=C+1:B=STICK(F+1):B2=STICK(F2):IF B=#FF THEN 3460
3485 IF B2<>#FF THEN 3460
3490 IF B<>D THEN 3460
3500 I=I+5
3510 POKE A,7:POKE P,K
3520 E=STICK(F+1):IF E<>#FF THEN 3520
3530 IF I<#482C THEN 3420
3535 Y=3:IF F=1 THEN Y=19
3540 LOCATE 0,17:PRINT BPC(60):LOCATE 6,17
3550 PRINT "HIT JOYSTICK SWITCH";D=0
3560 COLOR 2,0,1
3570 IF C=11 THEN LOCATE Y,3:PRINT A#;C=0:GOTO 3590
3580 IF C=6 THEN LOCATE Y,3:PRINT C#
3590 C=C+1:B=STICK(F+1):B2=STICK(F2):IF B=#FF THEN 3570
3595 IF B2<>#FF THEN 3570
3600 IF B<>#FF THEN 3570
3610 COLOR 7,0,1:LOCATE Y,3:PRINT A#
3620 E=STICK(F+1):IF E<>#FF THEN 3620
3630 COLOR 7,0,0:IF F=1:IF F2=1:IF F=2 THEN RETURN
3640 FOR J=1 TO 400:NEXT:GOTO 3270

```

## JR-200 TEST PROGRAM I/O TEST MEMORY DUMP

PAGE 1

PAGE : 2

## CHARACTERS

[illegible]

## CHARACTERS

4400	44	08	44	67	D0	00	00	00	00	7E	7E	7E	7E	7E	7E	7E	D.Dg...
4401	E0	90	E0	A0	97	05	05	07	00	E0	46	49	48	46	E1	09	O.F.O...
4410	E0	90	90	E4	04	07	04	04	00	60	90	80	90	67	02	02	...CFINF
4420	E0	90	90	E7	95	67	04	04	00	40	F0	50	02	0F	02	04	...r.g.
4430	E0	90	80	B7	E5	67	04	04	00	40	F0	50	02	0F	02	04	...r.g.
4440	E0	90	80	B7	E5	67	04	04	00	40	F0	50	02	0F	02	04	...r.g.
4450	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4460	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4470	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4480	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4490	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4500	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4510	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4520	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4530	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4540	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4550	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4560	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4570	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4580	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4590	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4600	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4610	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4620	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4630	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4640	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4650	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4660	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4670	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4680	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
4690	E0	90	F0	94	94	04	07	00	00	1B	24	42	7E	42	42	00	...r.g.
470																	

## CHARACTERS

5000	06	52	55	42	4F	55	54	71	02	07	00	00	01	BE	51	00	.RUBOUTq.....	
5100	01	51	77	04	45	00	00	01	BE	57	00	01	57	65	06	07	.GW.....W..Me..	
5200	00	00	01	BE	45	00	01	45	72	08	07	00	00	01	58	52	.EE..Er.....R	
5300	00	52	74	04	07	00	00	00	01	BE	54	00	01	54	79	00	.Rt.....T..Tv..	
5400	07	00	00	01	BE	59	00	01	55	75	0E	07	00	00	01	59	..Y..Yu.....	
5500	00	00	01	55	69	10	07	00	00	01	BE	49	00	01	49	6F	U..Ui.....I..Ib	
5600	12	07	00	00	01	BE	4F	00	01	4F	70	14	07	00	00	01	.....Op.....	
5700	BE	50	00	01	50	40	16	07	00	00	01	BE	40	00	01	40	.....P.....3..3	
5800	5B	18	07	00	00	01	BE	5B	00	01	5B	0D	1B	07	00	00	[.....I.....	
5900	07	BE	1F	00	00	01	BE	59	00	52	1F	1D	54	1F	1D	41	00	.....R..T..N..
6000	06	52	45	54	55	42	4E	61	03	09	00	00	01	BE	4E	00	.RETURNA.....A	
6100	01	73	05	09	00	00	00	00	BE	53	00	00	01	53	64	07	09	.As.....B.....Bd
6200	00	00	01	BE	44	00	00	01	44	66	09	09	00	00	01	BE	46	.....D..Dy.....
6300	00	01	46	67	0B	09	00	00	01	BE	47	00	01	47	6B	0D	.Fg.....3..Bh	
6400	09	00	00	01	BE	4B	00	00	01	4B	6A	0F	09	00	00	01	BE	.....H..Hj.....
6500	4A	00	01	4A	6B	11	09	00	00	01	BE	4B	00	01	4B	5C	J..Jk.....K..K1	



## JR-200 MEMORY DUMP V1.0

PAGE : 3

```

ADDR. 0 1 2 3 4 5 6 7 8 9 A B C D E F
4600 13 09 00 00 01 BE 4C 00 01 4C 3B 15 09 00 00 01
4610 BE 3B 00 01 3B 3A 17 09 00 00 01 BE 3A 00 01 3A
4620 5D 19 09 00 00 01 BE 5D 00 00 01 5D 7A 04 00 00 01
4630 01 BE 5A 00 01 5A 7B 06 08 00 00 01 BE 5B 00 01
4640 5B 63 0B 0B 00 01 BE 5C 00 01 43 76 0A 0B 00
4650 00 01 BE 56 00 01 56 62 0C 0B 00 01 BE 42 00
4660 01 42 6E 0E 0B 00 01 BE 4E 00 01 4E 6D 10 0B
4670 00 00 01 BE 4D 00 01 4D 2C 12 0B 00 01 BE 2C
4680 00 01 2C 2E 14 0B 00 01 BE 2E 00 01 2E 2F 16
4690 0B 00 00 01 BE 2F 00 01 2F 20 09 0D 00 0D BE
46A0 0E BE 0E BE BE BE BE BE BE BE BE BE BE BE BE BE BE BE
46B0 53 50 41 43 45 20 20 20 20 00 05 53 50 41 43 45
46C0 13 1D 07 00 01 01 F5 22 00 03 49 4E 53 7F 1E 07
46D0 02 01 01 F1 23 00 03 44 45 4C 1E 1E 09 02 00 01
46E0 F1 BB 00 01 BB 1D 1D 0B 00 00 01 F5 B6 00 01 B6
46F0 1C 1E 0B 02 00 01 F1 B9 00 01 B9 1F 1E 0D 02 00

```

CHARACTERS

```

ADDR. 0 1 2 3 4 5 6 7 8 9 A B C D E F
4700 01 F1 B7 00 01 B7 5A 01 0B 00 00 04 BE BE 1C BE
4710 53 49 1C 5A 02 05 53 48 49 46 54 5F 18 0B 00 00
4720 04 BE 1C BE BE 5F 1C 53 49 03 05 53 48 49 46 54
4730 FB 06 0B 00 01 04 BE 1F 1F BE 29 1F 1F 25 04 0B
4740 47 52 41 50 4B 20 4F 4E 7A 04 0B 00 01 04 BE 1F
4750 1F BE 2B 1F 1F 27 06 09 47 52 41 50 4B 20 4F 46
4760 46 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4770 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4780 00 00 47 BB 4B 17 C0 00 00 00 00 00 00 00 00
4790 07 1F 3F 7F 7F FF FF FF FF FF FF 7F 3F 1F 07
47A0 E0 FB FC FE FE FF FF FF FF FF FF FE FC FB FE
47B0 00 00 00 00 01 03 07 0F 00 00 00 7E FF FF FF
47C0 00 00 00 00 80 C0 E0 F0 0F 1F 1F 1F 1F 1F 0F
47D0 FF FF FF FF FF FF FF FF FF FF FB FB FB FB F0
47E0 0F 07 03 01 00 00 00 00 FF FF FF FF 7E 00 00
47F0 F0 E0 C0 B0 00 00 00 00 00 70 60 50 0B 04 02 00

```

CHARACTERS

```

ADDR. 0 1 2 3 4 5 6 7 8 9 A B C D E F
4800 00 0E 06 0A 10 20 40 00 00 02 04 0B 50 60 70 00
4810 00 40 20 10 0A 06 0E 00 C1 A7 BB 00 FE C1 E9 B9
4820 00 F7 C2 27 87 00 FD C1 E5 B6 00 FB 00 00 00 00
4830 40 C0 40 C2 C2 40 00 00 00 00 00 00 00 00 00
4840 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4850 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4860 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4870 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4880 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4890 00 00 00 00 00 00 00 00 00 00 00 00 00 00
48A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
48B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
48C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
48D0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
48E0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
48F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00

```

## JR-200 MEMORY DUMP V1.0

PAGE : 4

```

ADDR. 0 1 2 3 4 5 6 7 8 9 A B C D E F
4900 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4910 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4920 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4930 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4940 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4950 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4960 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4970 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4980 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4990 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
49A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
49B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
49C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
49D0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
49E0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
49F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

```

CHARACTERS

```

ADDR. 0 1 2 3 4 5 6 7 8 9 A B C D E F
4A00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4A10 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4A20 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4A30 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4A40 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4A50 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4A60 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4A70 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4A80 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4A90 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4AA0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4AB0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4AC0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4AD0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4AE0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4AF0 00 00 00 00 00 00 00 00 00 00 00 00 00 00

```

CHARACTERS

```

ADDR. 0 1 2 3 4 5 6 7 8 9 A B C D E F
4B00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4B10 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4B20 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4B30 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4B40 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4B50 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4B60 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4B70 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4B80 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4B90 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4BA0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4BB0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4BC0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4BD0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4BE0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4BF0 00 00 00 00 00 00 00 00 00 00 00 00 00 00

```

PAGE : 4

JR-200 MEMORY DUMP V1.0

PAGE : 5

JR-200 MEMORY DUMP V1.0

ADDR.	0	1	2	3	4	5	6	7	B	9	A	B	C	D	E	F	CHARACTERS
4F00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4F10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4F20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4F30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4F40	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4F50	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4F60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4F70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4F80	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4F90	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4FA0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4FB0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4FC0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4FD0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4FE0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
4FF0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
ADDR.	0	1	2	3	4	5	6	7	B	9	A	B	C	D	E	F	CHARACTERS
5000	30	00	18	00	18	00	F0	29	18	00	18	00	18	00	18	00	0.....
5010	24	00	0C	1B	18	00	18	00	18	16	18	00	30	00	18	14	.....
5020	18	00	30	00	18	16	18	00	30	00	24	19	0C	00	18	00	.....
5030	18	17	18	00	18	00	30	19	30	00	30	00	18	16	48	00	.....
5040	24	00	0C	1B	18	00	18	00	18	16	18	00	30	00	18	14	.....
5050	18	00	30	00	18	16	18	00	30	00	24	19	0C	00	18	00	.....
5060	18	17	18	00	18	00	30	19	30	00	30	00	18	16	48	00	.....
5070	30	00	30	00	30	00	18	00	18	00	F0	00	C0	00	18	0F	.....
5080	18	00	2D	00	03	00	15	00	03	00	15	18	03	00	30	00	.....
5090	18	16	18	00	18	00	48	14	30	00	18	00	18	14	30	00	.....
50A0	18	00	18	18	30	00	18	00	18	18	60	00	30	00	18	1B	.....
50B0	18	00	2D	00	03	00	18	00	18	00	30	14	18	00	18	00	.....
50C0	18	1B	48	00	30	00	18	11	18	00	30	00	18	13	18	00	.....
50D0	30	00	18	18	00	60	00	00	30	00	30	00	30	00	24	19	.....
50E0	0C	00	18	00	18	17	18	00	18	00	30	19	18	00	18	00	.....
50F0	30	17	18	00	18	00	30	19	24	00	0C	00	18	19	18	00	.....
ADDR.	0	1	2	3	4	5	6	7	B	9	A	B	C	D	E	F	CHARACTERS
5100	18	00	18	17	30	00	30	00	30	17	18	00	48	00	30	00	.....
5110	30	00	30	00	18	29	18	00	F0	00	D0	00	48	00	18	00	.....
5120	24	14	0C	00	24	00	0C	16	60	00	60	00	2D	19	03	00	.....
5130	30	00	30	14	30	00	90	00	30	00	48	00	18	00	24	14	.....
5140	0C	00	24	00	0C	16	60	00	60	00	2D	16	03	00	2D	00	.....
5150	03	00	30	00	30	00	90	16	30	00	45	00	03	00	18	00	.....
5160	24	00	0C	16	24	00	0C	00	60	14	60	00	2D	00	03	00	.....
5170	30	00	30	00	30	16	90	00	30	00	48	11	18	00	24	00	.....
5180	0C	13	24	00	0C	00	45	0F	03	00	18	00	60	14	48	00	.....
5190	18	00	30	18	30	00	90	00	30	00	22	00	02	00	0A	0F	.....
51A0	02	00	22	00	02	00	0C	00	48	00	18	13	22	00	02	00	.....
51B0	0A	11	02	00	22	00	02	00	0C	00	48	00	18	14	22	00	.....
51C0	02	00	0A	13	02	00	22	00	02	00	0C	00	30	00	30	13	.....
51D0	30	00	30	00	60	18	22	00	02	00	0A	0F	02	00	22	00	.....
51E0	02	00	0C	00	48	00	18	13	22	00	02	00	0A	11	02	00	.....
51F0	22	00	02	00	0C	00	48	00	18	14	22	00	02	00	0A	13	.....

## JR-200 MEMORY DUMP V1.0

PAGE 1 7

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
5200	02	00	22	00	02	00	0C	00	30	00	30	13	90	00	30	00	".....O.O..r.O..
5210	30	00	30	00	18	00	1B	00	F0	00	00	00	00	00	00	00	O.O.....J)9.9..r
5220	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5230	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5240	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5250	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5260	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5270	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5280	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5290	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
52A0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
52B0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
52C0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
52D0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
52E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
52F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
-------	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	------------

5300	30	00	1B	29	1B	00	F0	00	1B	00	1B	00	1B	00	1B	00	O.).....J.....
5310	24	00	0C	00	1B	19	1B	00	1B	00	1B	17	30	00	1B	00	\$.....O.....
5320	1B	16	30	00	1B	00	1B	17	30	00	24	00	0C	1B	1B	00	O.....O.....
5330	1B	00	1B	16	1B	00	30	00	30	14	30	00	1B	00	4B	12	.....O.O.....H.
5340	24	00	0C	00	1B	19	1B	00	1B	00	1B	17	30	00	1B	00	\$.....O.....
5350	1B	16	30	00	1B	00	1B	17	30	00	24	00	0C	1B	1B	00	.....O.....
5360	1B	00	1B	16	1B	00	30	00	30	14	30	00	1B	00	4B	12	.....O.O.....H.
5370	30	00	30	00	30	00	1B	00	1B	00	F0	29	00	00	1B	00	O.O.....J)9..
5380	1B	14	2D	00	03	00	1B	00	03	00	15	00	00	00	30	1B	.....O.....
5390	1B	00	1B	1B	00	4B	00	30	00	1B	00	1B	00	1B	00	30	.....H.O.....
53A0	1B	00	1B	00	30	1B	1B	00	1B	00	60	16	30	00	1B	00	.....O.....
53B0	1B	19	2D	00	03	00	1B	1B	1B	00	30	00	1B	16	1B	00	.....O.....
53C0	1B	00	4B	19	30	00	1B	00	1B	10	30	00	1B	00	1B	14	.....H.O.....
53D0	30	00	1B	00	1B	16	60	00	30	00	30	00	30	00	24	00	O.....O.O.O.\$.
53E0	0C	1B	1B	00	1B	00	1B	16	1B	00	30	00	1B	14	1B	00	.....O.....
53F0	30	00	1B	16	1B	00	30	00	24	19	0C	00	1B	00	1B	17	O.....O.\$.....

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
-------	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	------------

5400	1B	00	1B	00	30	19	30	00	30	00	1B	16	4B	00	30	00	.....O.O.....H.O.
5410	30	00	30	00	1B	00	1B	00	F0	00	00	00	4B	14	1B	00	O.O.....J)9.H..
5420	24	00	0C	0F	24	00	0C	00	60	1B	60	00	2D	00	03	00	\$.....J)9.H..
5430	30	00	30	00	30	16	90	00	30	00	4B	14	1B	00	24	00	O.O..r.O.H..\$.
5440	0C	0F	24	00	0C	00	60	1B	60	00	2D	00	03	00	2D	00	\$.....J)9.H..
5450	03	00	30	16	30	00	90	00	30	00	45	00	03	00	1B	16	.....O.O..r.O.E..
5460	24	00	0C	00	24	1B	0C	00	60	00	60	0F	2D	00	03	00	\$.....J)9.H..
5470	30	19	30	00	30	00	90	1B	30	00	4B	00	1B	13	24	00	O.O..r.O.H..\$.
5480	0C	00	24	14	0C	00	45	00	03	00	1B	00	60	00	4B	1B	\$.....E.....H.
5490	1B	00	30	00	30	16	90	00	30	00	22	0F	02	00	0A	00	.....O.O..r.O..
54A0	02	00	22	00	02	00	0C	0F	4B	00	1B	00	22	11	02	00	.....H.....
54B0	0A	00	02	00	22	00	02	00	0C	11	4B	00	1B	00	22	13	.....H.....
54C0	0A	00	0A	00	02	00	22	00	02	00	0C	13	30	00	30	00	.....H.....
54D0	30	14	30	00	60	00	22	0F	02	00	0A	00	02	00	22	00	O.O..r.O..
54E0	02	00	0C	0F	4B	00	1B	00	22	11	02	00	0A	00	02	00	.....H.....
54F0	22	00	02	00	0C	11	4B	00	1B	00	22	13	02	00	0A	00	.....H.....

## JR-200 MEMORY DUMP V1.0

PAGE 1 8

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
5500	02	00	22	00	02	00	0C	13	30	00	30	00	90	14	30	00	".....O.O..r.O..
5510	30	00	30	00	1B	00	1B	00	F0	29	00	00	00	00	00	00	O.O.....J)9.9..r
5520	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5530	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5540	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5550	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5560	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5570	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5580	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5590	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
55A0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
55B0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
55C0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
55D0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
55E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
55F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
-------	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	------------

5600	30	00	1B	00	1B	00	F0	00	1B	00	1B	00	1B	00	1B	00	O.....J.....
5610	24	19	0C	00	1B	00	1B	17	1B	00	1B	00	30	19	1B	00	\$.....O.....
5620	1B	00	30	17	1B	00	1B	00	30	19	24	00	0C	00	1B	19	O.....O.\$.....
5630	1B	00	1B	00	1B	17	30	00	30	00	30	19	1B	00	4B	00	.....O.O.....H.
5640	24	19	0C	00	1B	00	1B	17	1B	00	1B	00	30	19	1B	00	\$.....O.....
5650	1B	00	30	17	1B	00	1B	00	30	19	24	00	0C	00	1B	19	O.....O.\$.....
5660	1B	00	1B	00	1B	17	30	00	30	00	30	19	1B	00	4B	00	.....O.O.....H.
5670	30	00	30	00	30	00	1B	29	1B	00	F0	00	00	00	1B	00	O.O..r.O..J)9..
5680	1B	00	2D	1B	03	00	15	00	03	00	15	00	00	00	30	1B	.....O.....
5690	1B	00	1B	00	1B	16	4B	00	30	00	1B	0F	1B	00	30	00	.....H.O.....
56A0	1B	14	1B	00	30	00	1B	19	1B	00	60	00	30	00	1B	00	.....O.....
56B0	1B	00	2D	1B	03	00	1B	00	1B	16	30	00	1B	00	1B	00	.....O.....
56C0	1B	00	4B	00	30	00	1B	00	1B	00	30	0F	1B	00	1B	00	.....H.O.....
56D0	30	16	1B	00	1B	00	60	14	30	00	30	00	30	00	24	00	O.....O.O.O.\$.
56E0	0C	00	1B	19	1B	00	1B	00	1B	17	30	00	1B	00	1B	16	.....O.....
56F0	30	00	1B	00	1B	17	30	00	24	00	0C	1B	00	1B	00	1B	O.....O.\$.....

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
-------	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	------------

5700	1B	16	1B	00	30	00	30	14	30	00	1B	00	4B	12	30	00	.....O.O.....H.O.
5710	30	00	30	00	1B	00	1B	00	F0	29	00	00	4B	00	1B	0F	O.O.....J)9.H..
5720	24	00	0C	00	24	14	0C	00	60	60	60	14	2D	00	03	00	0.....J)9.H..
5730	30	19	30	30	00	90	1B		30	00	4B	00	1B	0F	24	00	0.....J)9.H..
5740	0C	00	24	14	0C	60	00		60	14	2D	00	03	00	2D	16	0.....J)9.H..
5750	03	00	30	30	30	1B	90	00	30	00	45	16	03	00	1B	00	0.....J)9.H..
5760	24	15	0C	00	24	00	0C	16	60	60	60	2D	19	03	00		0.....J)9.H..
5770	30	00	30	14	30	00	90	00	30	00	4B	00	1B	00	24	14	0.....J)9.H..
5780	0C	00	24	00	0C	11	45	00	03	00	1B	0F	60	00	4B	00	0.....J)9.H..
5790	1B	19	30	30	00	90	14		30	00	22	00	02	00	0A	00	0.....J)9.H..
57A0	02	00	22	0F	02	00	0C	00	4B	14	1B	00	02	00	0A	00	0.....J)9.H..
57B0	0A	00	02	00	22	11	02	00	0C	00	4B	16	1B	00	22	00	0.....J)9.H..
57C0	02	00	0A	00	02	11	02	00	02	00	0C	00	30	11	30	00	0.....J)9.H..
57D0	30	00	30	16	60	00	22	00	02	00	0A	00	02	00	22	0F	0.....J)9.H..
57E0	22	11	02	00	0C	4B	14	1B	00	22	00	02	00	0A	00	00	0.....J)9.H..
57F0	02	00	0C	00	00	4B	16		1B	00	22	00	02	00	0A	00	0.....J)9.H..

PAGE : 10

JR-200 MEMORY DUMP V1.0

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
5B00	00	00	00	00	00	00	00	00	00	00	03	03	00	00	00	00	.....
5B10	00	00	00	03	03	03	00	00	00	00	00	00	00	00	00	00	.....
5B20	00	00	00	00	00	00	00	00	00	00	03	00	00	00	00	00	.....
5B30	00	00	00	03	00	03	00	00	00	00	00	00	00	00	00	00	.....
5B40	00	00	00	00	00	00	00	00	00	00	01	01	01	01	00	01	.....
5B50	00	00	01	01	01	01	01	00	00	00	00	00	00	00	00	00	.....
5B60	00	00	00	00	00	00	00	00	02	01	01	01	01	03	00	01	.....
5B70	00	02	01	01	01	03	01	00	00	00	00	00	00	00	00	00	.....
5B80	00	00	00	00	00	00	00	00	01	00	01	00	03	03	01	00	.....
5B90	01	00	01	01	00	01	00	00	00	00	00	00	00	00	00	00	.....
5BA0	00	00	00	00	00	00	00	00	00	01	00	01	01	01	01	01	.....
5BB0	01	01	00	01	01	00	01	00	00	00	00	00	00	00	00	00	.....
5BC0	00	00	00	00	00	00	00	00	00	00	03	00	00	03	00	00	.....
5BD0	00	00	00	00	03	00	00	00	00	00	00	00	00	00	00	00	.....
5BE0	00	00	00	00	00	00	00	00	00	00	03	03	03	03	00	00	.....
5BF0	00	00	00	00	03	03	00	00	00	00	00	00	00	00	00	00	.....

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
5C00	00	00	00	00	00	00	00	00	00	00	00	03	03	03	00	00	.....
5C10	00	00	00	03	03	00	00	00	00	00	00	00	00	00	00	00	.....
5C20	00	00	00	00	00	00	00	00	00	00	00	00	00	03	03	02	.....
5C30	02	03	03	03	00	00	00	00	00	00	00	00	00	00	00	00	.....
5C40	00	00	00	00	00	00	00	00	00	00	00	00	00	00	03	03	.....
5C50	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5C60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5C70	03	03	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5C80	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5C90	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5CA0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5CB0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5CC0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5CD0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5CE0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5CF0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
5D00	00	01	01	02	02	03	03	04	04	05	05	04	06	07	07	00	.....
5D10	00	02	01	03	02	04	03	05	04	06	05	07	06	00	07	01	.....
5D20	00	03	01	04	02	05	03	06	04	07	05	00	06	01	07	02	.....
5D30	00	04	01	05	02	06	00	07	04	00	05	01	06	02	07	03	.....
5D40	00	05	01	06	02	07	03	00	04	01	05	02	06	03	07	04	.....
5D50	00	06	01	07	02	00	03	01	04	02	05	03	06	04	07	05	.....
5D60	00	07	01	00	02	01	03	02	04	03	05	04	06	05	00	06	.....
5D70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5D80	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5D90	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5DA0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5DB0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5DC0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5DD0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5DE0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5DF0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....

PAGE : 9

JR-200 MEMORY DUMP V1.0

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
5B00	02	00	22	13	02	00	0C	00	30	11	30	00	90	00	30	00	.....
5B10	30	00	30	00	1B	29	1B	00	F0	00	00	00	00	00	FE	00	.....
5B20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5B30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5B40	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5B50	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5B60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5B70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5B80	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5B90	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5BA0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5BB0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5BC0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5BD0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5BE0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5BF0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
5900	20	20	20	20	20	20	20	20	BE	BE	BE	B2	B1	B0	BE	BE	.....
5910	BE	BE	BE	19	18	BE	BE	BE	20	20	20	20	20	20	20	20	.....
5920	20	20	20	20	20	20	20	20	BE	BE	BE	BE	1F	1E	1D	92	.....
5930	92	1C	1B	1A	BE	BE	BE	BE	20	20	20	20	20	20	20	20	.....
5940	BE	BE	BE	BE	BE	BE	BE	BE	BE	BE	BE	BE	BE	BE	BE	01	.....
5950	20	20	20	20	20	20	20	20	BE	BE	BE	BE	BE	BE	BE	20	.....
5960	20	20	20	20	20	20	20	20	BE	BE	BE	BE	BE	BE	BE	20	.....
5970	00	01	BE	BE	BE	BE	BE	BE	20	20	20	20	20	20	20	20	.....
5980	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	.....
5990	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	.....
59A0	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	.....
59B0	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	.....
59C0	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	.....
59D0	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	.....
59E0	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	.....
59F0	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	.....

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
5A00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5A10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5A20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5A30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5A40	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
5A50	00	00	00	00	00</												

## JUN-200 MEMORY DUMP V1.0

PAGE : 11

JR-200 MEMORY DUMP V1.0

PAGE : 12

[illegible]

## CHARACTERS

[illegible]

## CHARACTERS

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
6200	08	8C	C2	80	26	FB	86	20	A7	00	08	8C	C4	00	26	F8
6210	5F	4F	DE	CB	00	FF	68	3E	CE	C5	00	FF	68	40	A7	00
6220	20	01	A7	02	A7	03	FF	68	42	67	68	44	B6	48	43	8B
6230	A0	24	03	7C	68	42	B7	68	43	FE	68	42	BC	68	3E	27
6240	05	B6	68	40	20	D8	B6	68	2F	8B	04	24	03	7C	68	3E
6250	87	B6	3F	B6	68	41	B8	04	34	03	7C	68	40	B7	68	41
6260	B6	68	44	04	B8	09	81	48	27	05	FE	68	40	20	B0	39
6270	01	01	01	01	01	01	01	DE	C5	00	B6	07	A7	00	08	CB
6280	00	26	F8	7F	68	45	DE	40	DC	FF	68	46	A6	02	E6	03
6290	B6	68	47	F7	68	49	EE	00	F1	68	4A	B6	00	A7	00	08
62A0	87	9B	C6	01	A7	00	08	5C	F1	68	48	26	F7	09	B6	8D
62B0	40	0F	68	4A	C6	01	B6	68	48	B8	20	24	03	7C	68	68
62C0	A4	B7	68	4B	FE	68	4A	B6	9A	A7	00	5C	F1	68	49	26
62D0	E6	FE	68	4A	B6	F0	A7	00	09	C6	01	B6	9A	A7	00	08
62E0	5C	F1	68	4B	26	F7	08	B6	EF	A7	00	FF	68	4A	C6	01
62F0	B6	68	4B	80	20	24	03	7A	68	4A	B7	68	48	FE	68	4A

## CHARACTERS

[illegible]

## CHARACTERS

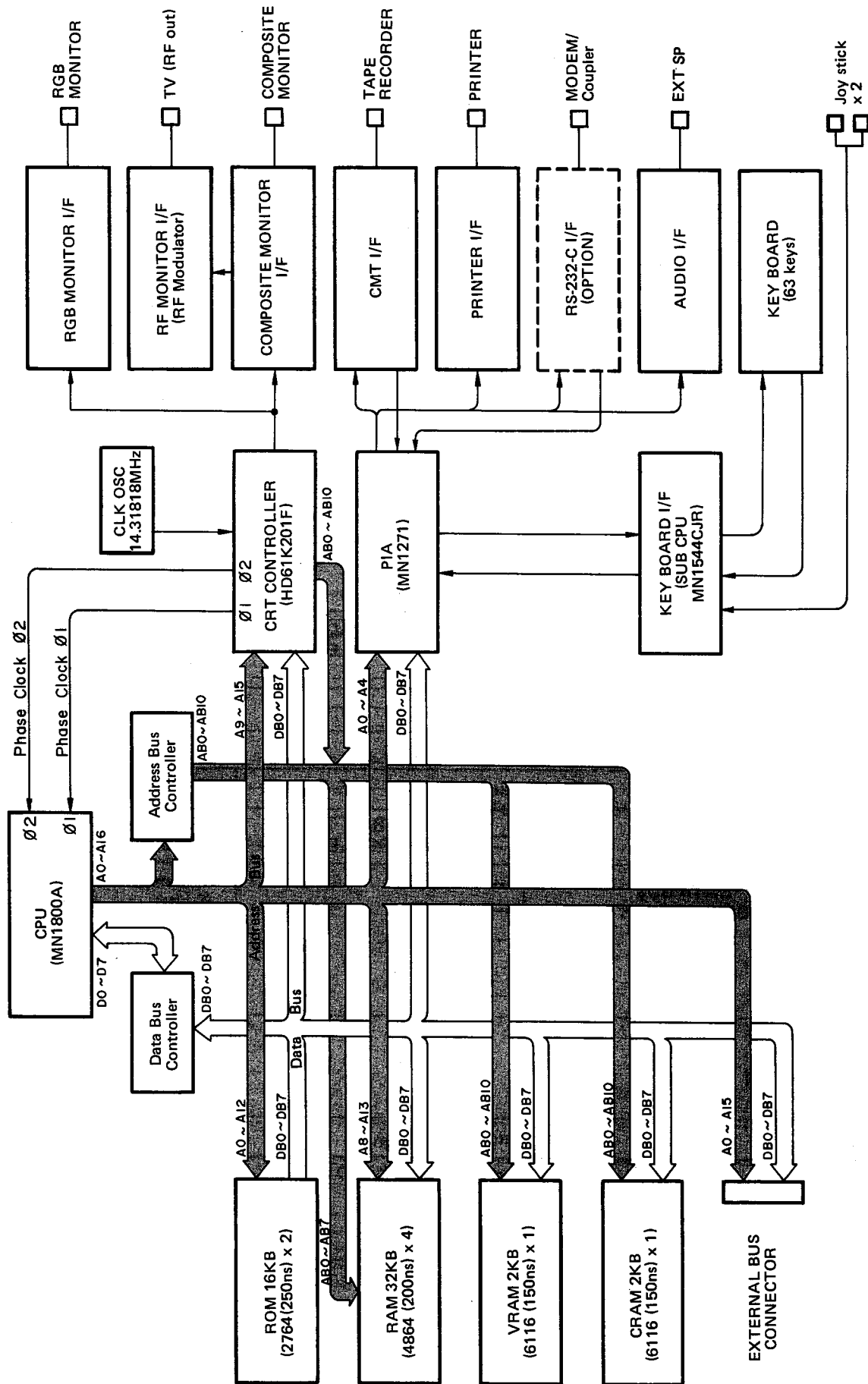
ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
5300	B6	9A	A7	00	5C	F1	6B	49	26	E6	B6	90	A7	00	FE	6B
5310	46	0B	08	08	FF	68	46	49	B6	68	45	4C	B7	6B	45	81
5320	04	27	03	7E	62	B9	39	01	01	01	01	01	01	CE	C1	00
5330	B6	B9	A7	00	0B	8C	C4	00	26	F8	CE	C5	00	B6	BF	A7
5340	08	8C	C8	00	06	F8	39	01	01	01	01	01	01	01	CE	C0
5350	00	A7	00	08	8C	C1	00	26	F8	CE	C4	00	A7	00	0B	8C
5360	C5	00	26	F8	CE	C5	00	C6	E7	00	08	8C	C8	00	26	C4
5370	F8	B1	00	27	05	BD	63	7E	20	03	BD	63	98	39	CE	C1
5380	00	B8	00	A7	00	8C	C4	00	CE	00	F8	CE	40	EC	BD	64
5390	08	CE	40	F8	BD	64	08	39	CE	C1	00	B6	BE	A7	00	0B
53A0	8C	C4	00	26	F8	CE	40	F2	BD	64	08	CE	40	F8	BD	64
53B0	08	39	01	01	01	01	01	01	01	01	01	01	01	01	01	01
53C0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
53D0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
53E0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	CE	C1
53F0	00	4F	A7	00	0B	8C	C4	00	26	F8	CE	C5	00	B6	07	A7

JR-200 MEMORY DUMP V1.0

PAGE : 13

ADDR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHARACTERS
6400	00	08	BC	C8	00	26	F8	39	36	37	FF	68	00	B6	68	00	..
6410	F6	68	01	36	37	EE	00	FF	68	02	FE	68	00	EE	04	FF	h.67
6420	68	04	FE	68	00	EE	02	08	FF	68	06	FE	68	02	A6	00	h.h.
6430	08	FF	68	02	FE	68	04	A7	00	08	FF	68	04	FE	68	02	h.h.
6440	BC	68	06	26	E6	33	32	F7	68	01	B7	68	00	FE	68	00	h.h.
6450	33	32	39	01	01	01	01	01	01	01	01	01	01	01	01	01	h.h.
6460	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	h.h.
6470	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	h.h.
6480	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	h.h.
6490	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	h.h.
64A0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	h.h.
64B0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	h.h.
64C0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	h.h.
64D0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	h.h.
64E0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	h.h.
64F0	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	h.h.

## 2. Block Diagram



### 3. Signal Code Table

#### 3.1. Address Bus Singals

Signal Code	Direction		Function
A0 to A15	CPU		CPU Address bus signal. (16 bits)
AB0 to AB10	CRTC		CRTC Address bus signal for CRT display. (AB0 to AB10)
	CRTC		CRTC Address bus signal for Memory RAS—only refresh. (AB0 to AB6)
	ADDRESS BUS CONTROLLER		CPU Address bus signal controlled by O <sub>2</sub> S signal. (AB0 to AB10)
MA0 to MA7	MEMORY ADDRESS CONTROLLER		8 bits Address bus signal.
E0, E1	CRTC		2 bits external Address bus signal created by CRTC for Memory controll.

#### 3.2. Data Bus Singals

Signal Code	Direction		Function
D0 to D7	CPU		CPU Data bus signal. (8 bits)
DB0 to DB7	DATA BUS CONTROLLER		System Data bus signal. (8 bits)

#### 3.3. Sub CPU

Signal Code	Direction		Function
KST0 to KST9	SUB CPU		Key strobe signal. (KST0 to KST7) Joystick strobe signal. (KST8, KST9)
KIN0 to KIN7	KEYBOARD JOYSTICK		Key-in signal. (KIN0 to KIN7) Joystick-on signal. (KIN0 to KIN5)
KD0 to KD7	SUB CPU		Key Code Data signal. (8 bits)



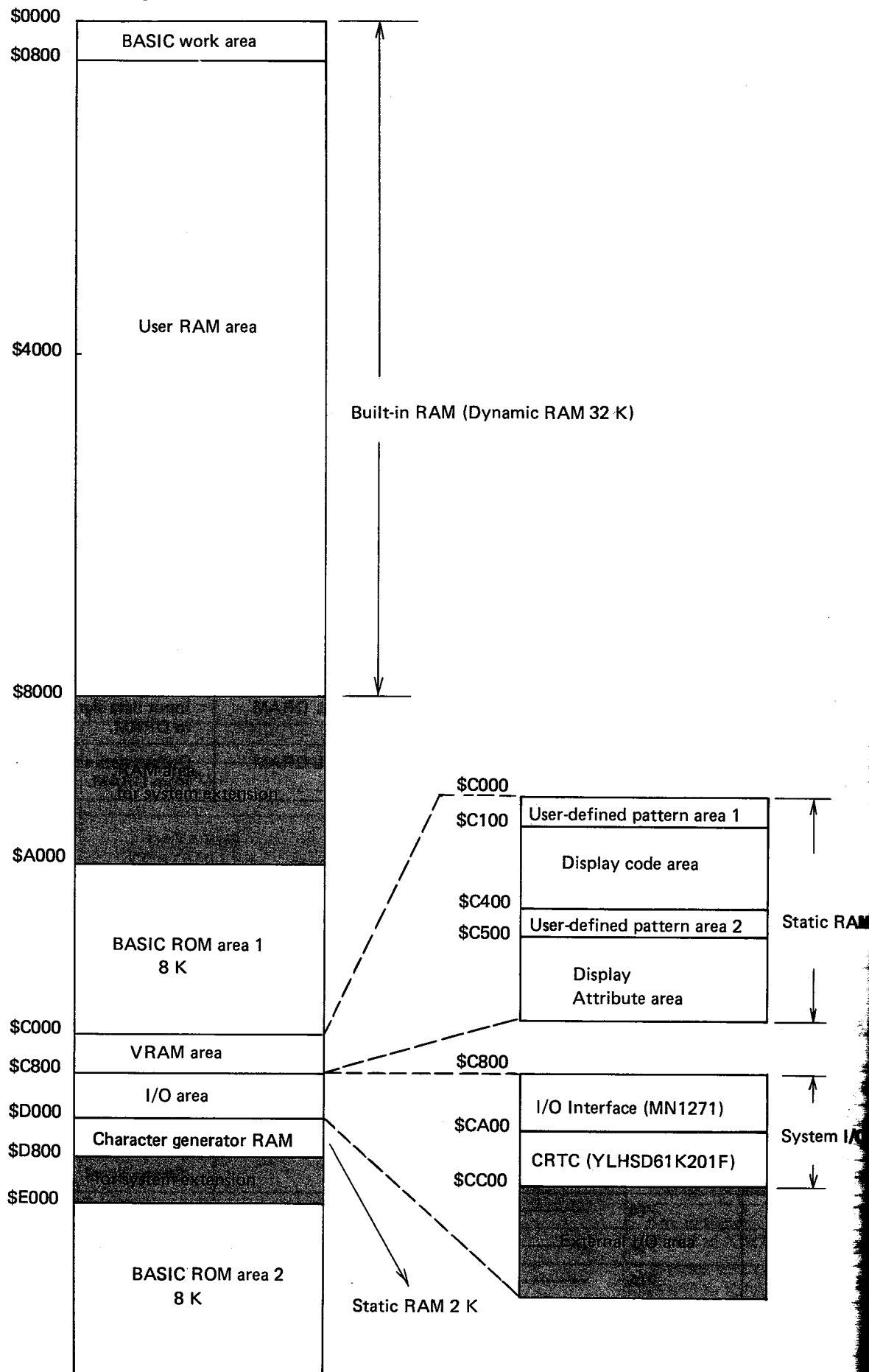
### 3.4. External Bus

Signal Code	Direction		Function
$\overline{E}\phi_2$	CRTC	→ EXTERNAL EQUIPMENT	CPU clock $\phi_2$
$\overline{E}O_2S$	CRTC	→ EXTERNAL EQUIPMENT	Clock for peripheral chips.
$\overline{ER}/\overline{W}$	CPU	→ EXTERNAL EQUIPMENT	CPU Read/Write signal.
$\overline{VMA}$	CPU	→ EXTERNAL EQUIPMENT	Valid memory address signal.
$\overline{ERESET}$	POWER ON RESET CIRCUIT	→ EXTERNAL EQUIPMENT	System reset signal.
$\overline{SYSINT}$	PIA	← EXTERNAL EQUIPMENT	System interrupt signal.
$\overline{USERINT}$	PIA	← EXTERNAL EQUIPMENT	User interrupt signal.
$\overline{KILL}$	CPTC	← EXTERNAL EQUIPMENT	ROM0 (IC5) kill signal.
$\overline{DRAMSEL}$	CRTC	← EXTERNAL DRAM	RAM Select signal.
$\overline{RAS}$	CRTC	→ EXTERNAL DRAM	RAS timing signal for DRAM.
$\overline{TCAS}$	CRTC	→ EXTERNAL DRAM	CAS timing signal for DRAM.
$\overline{ADSEL}$	CRTC	→ EXTERNAL DRAM	Memory address select signal.
$\overline{DRAM\phi IN}$ $\overline{DRAM1 IN}$	CRTC	→ EXTERNAL DRAM	Input data signal to DRAM.
$\overline{DRAM\phi OUT}$ $\overline{DRAM1 OUT}$	CRTC	← EXTERNAL DRAM	Output data signal from DRAM.

### 3.5. Printer Interface

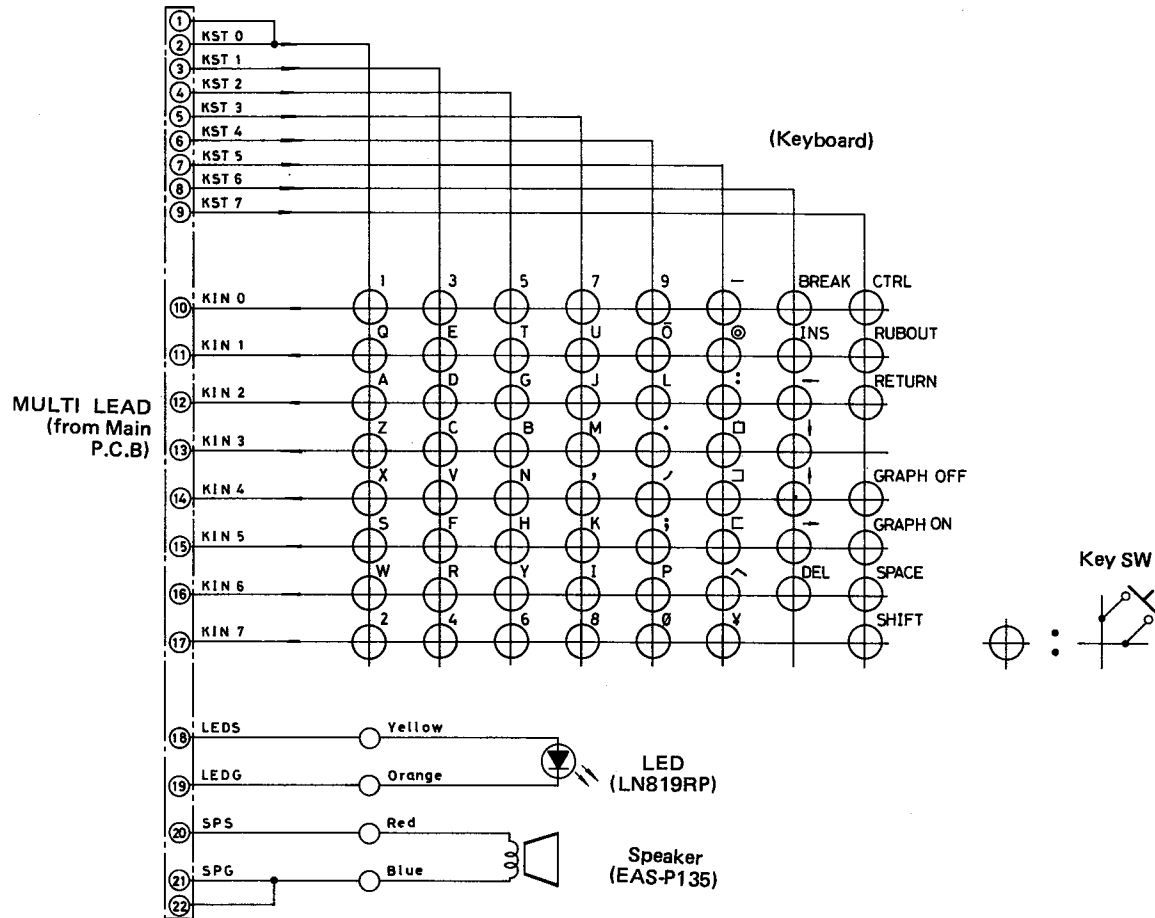
Signal Code	Direction		Function
PDATA0 to PDATA7	PIA	→ PRINTER	Data bus signal to printer.
STROBE	PIA	→ PRINTER	Strobe signal.
INITIAL	PIA	→ PRINTER	PRINTER reset signal.
BUSY	PIA	← PRINTER	Busy signal to system.
PSEL	PIA	← PRINTER	PRINTER select signal.

## 4. Memory Map



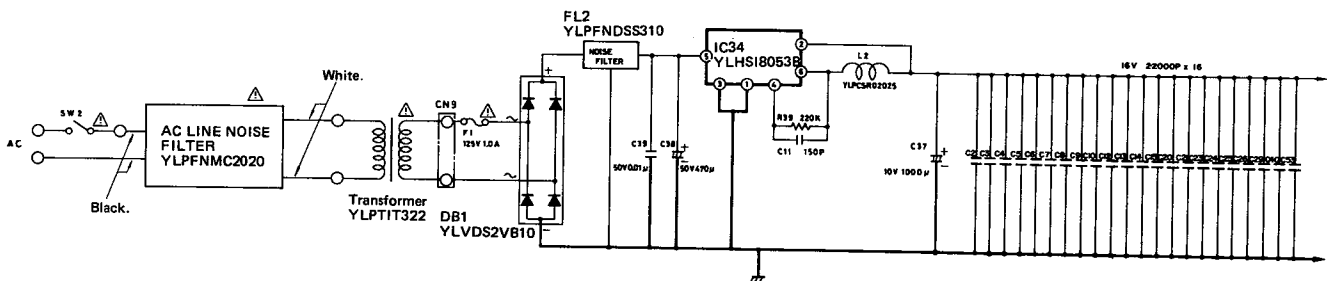
## 5. Schematic Diagram

### 5.1. Power Supply and Keyboard

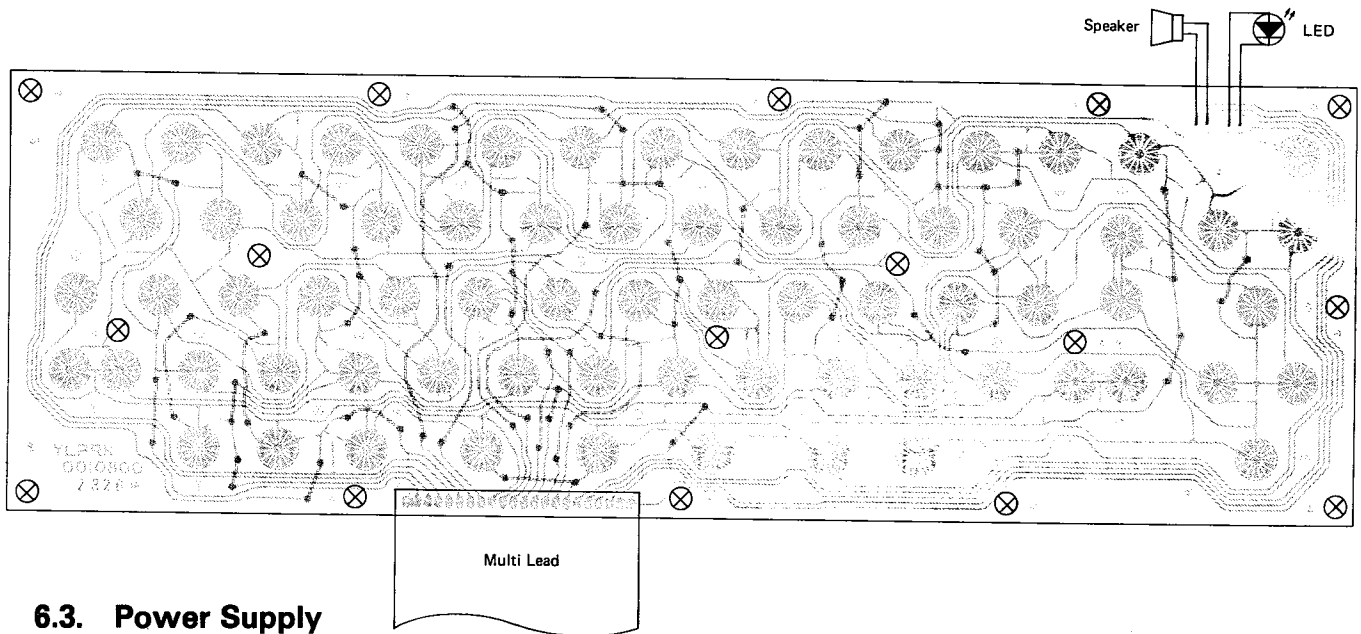


Power Supply Block

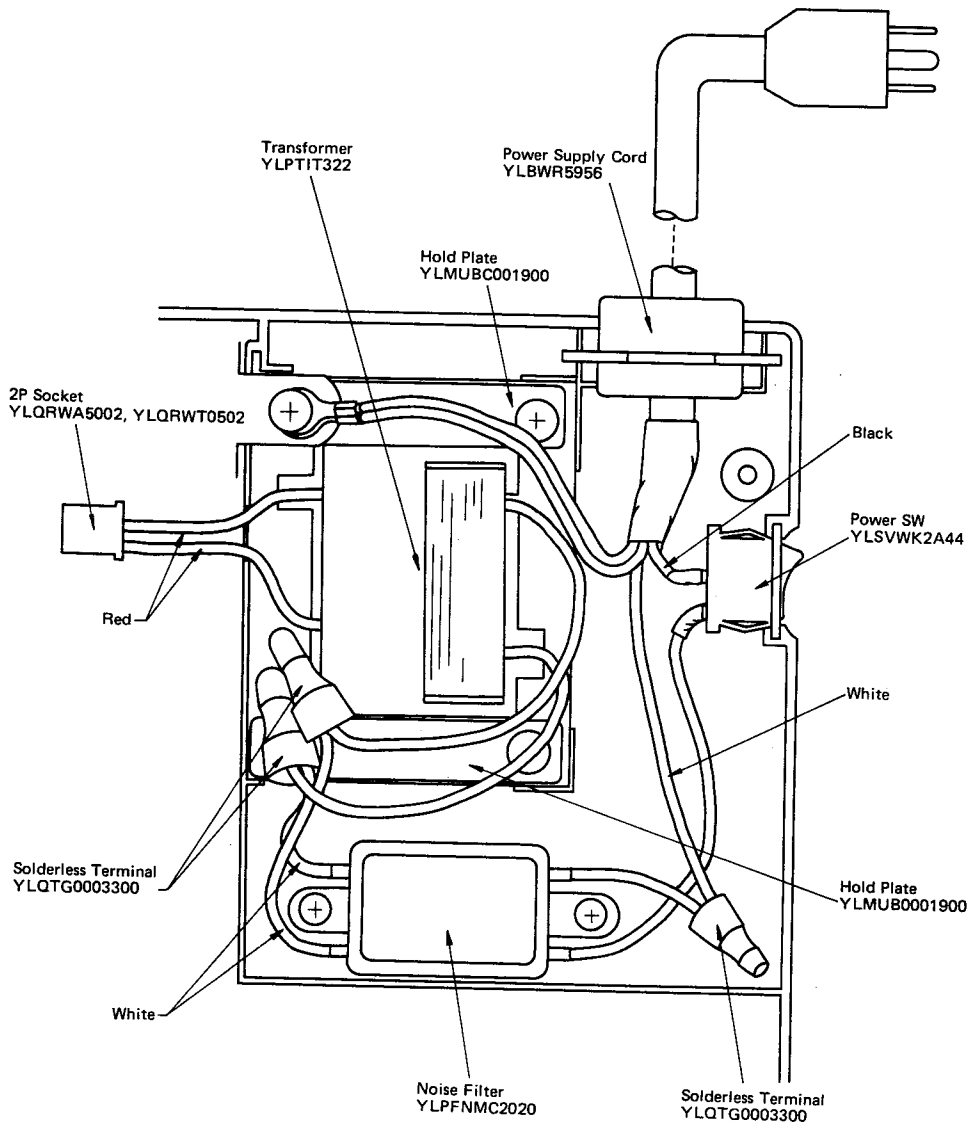
Main P.C.B.



## 6.2. Keyboard

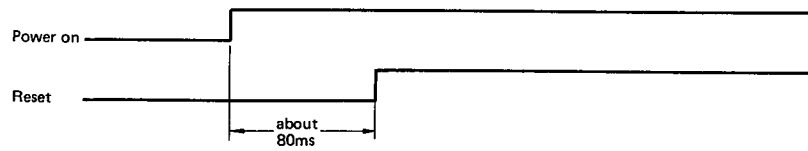


## 6.3. Power Supply

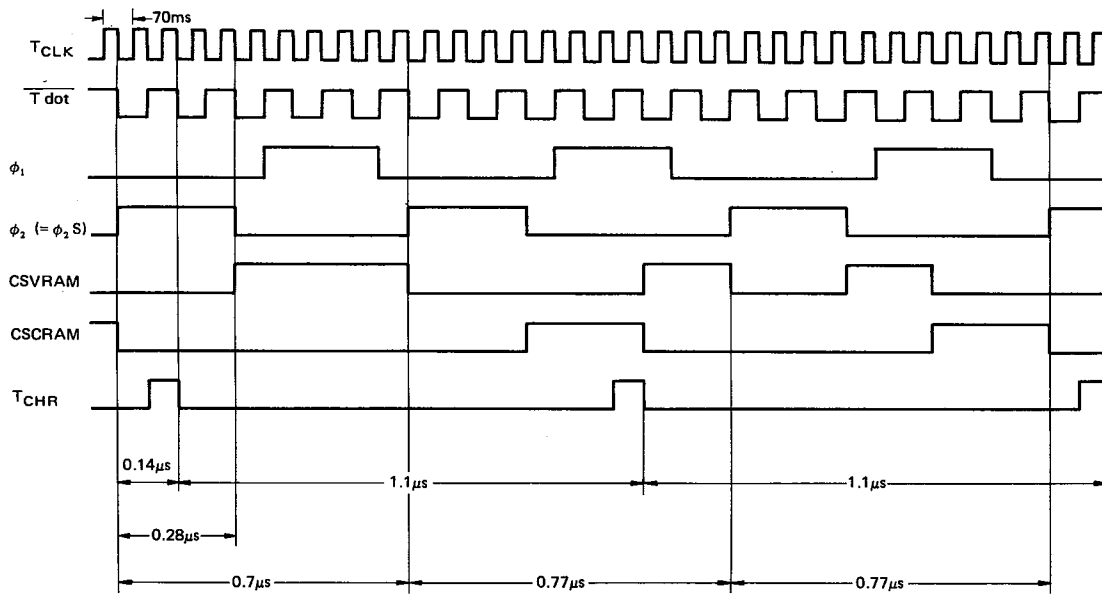


## 7. Waveforms

### 7.1. Power On Reset Timing

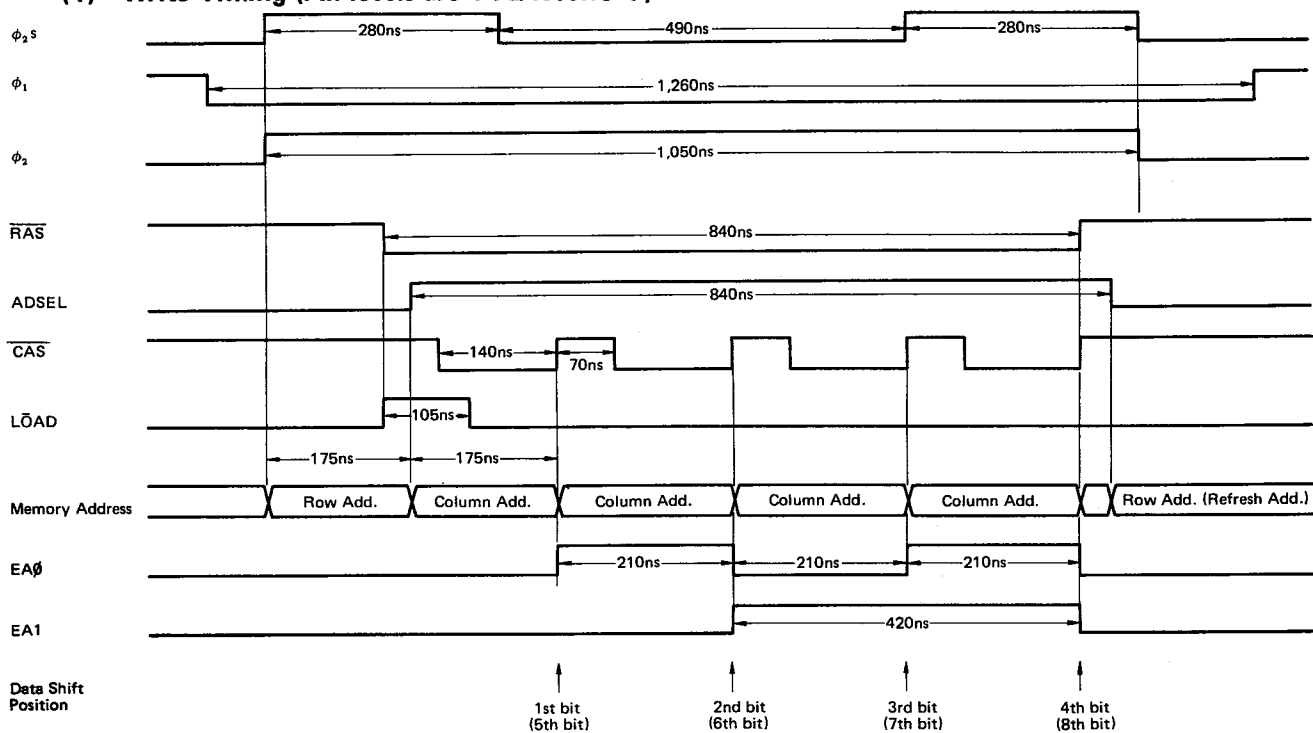


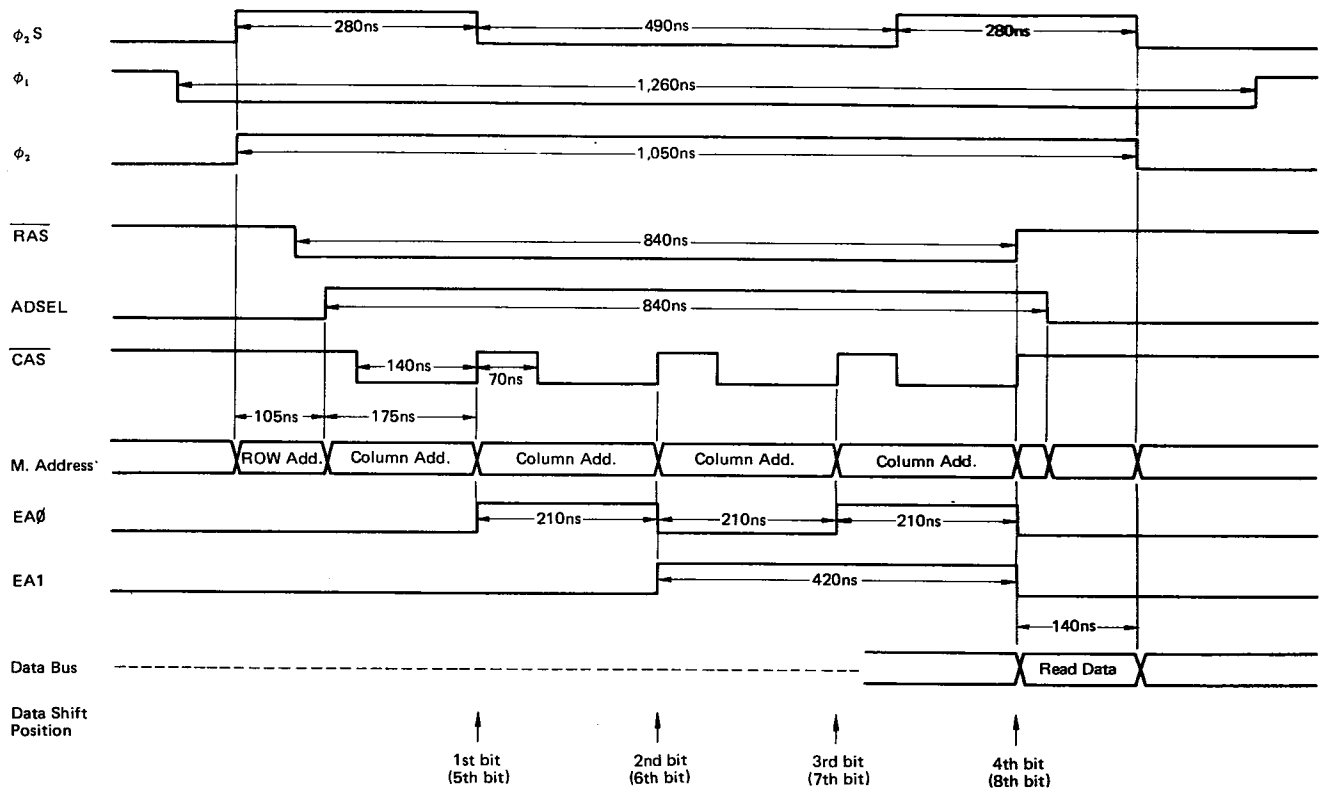
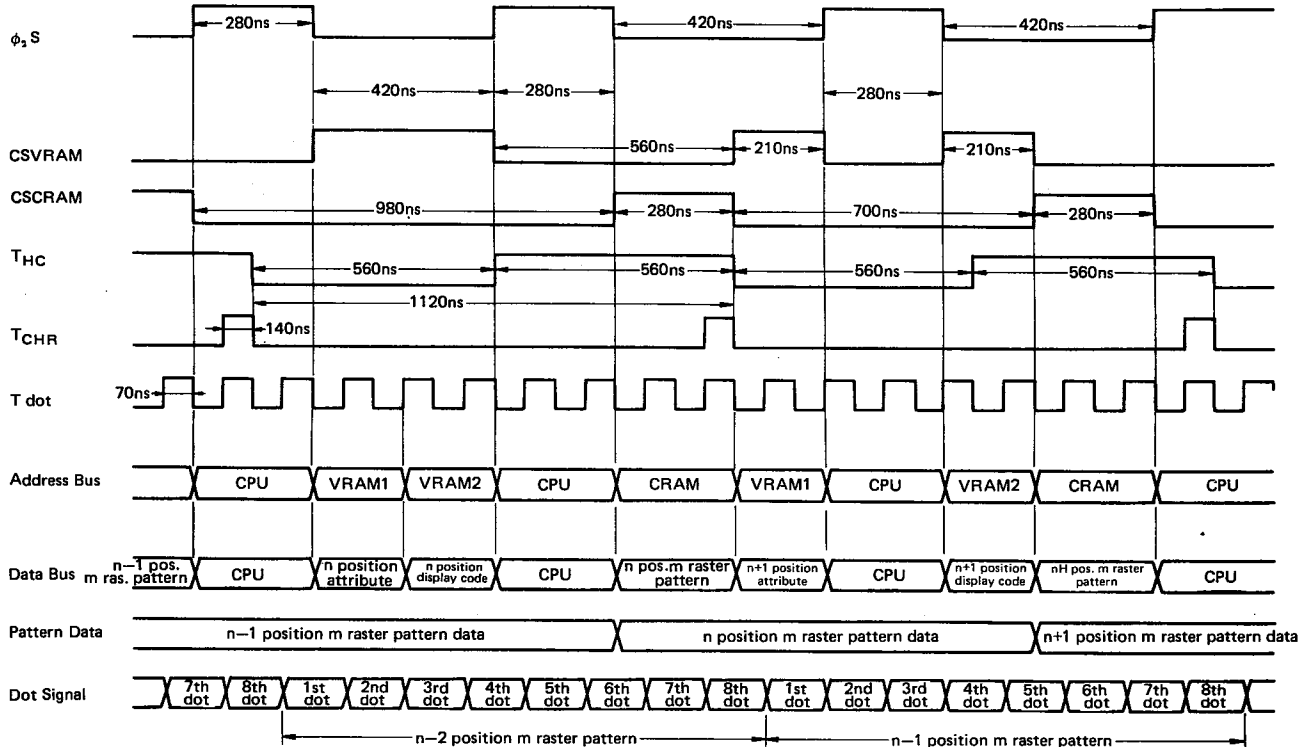
### 7.2. Basic Timing (See levels are TTL level:5 V)



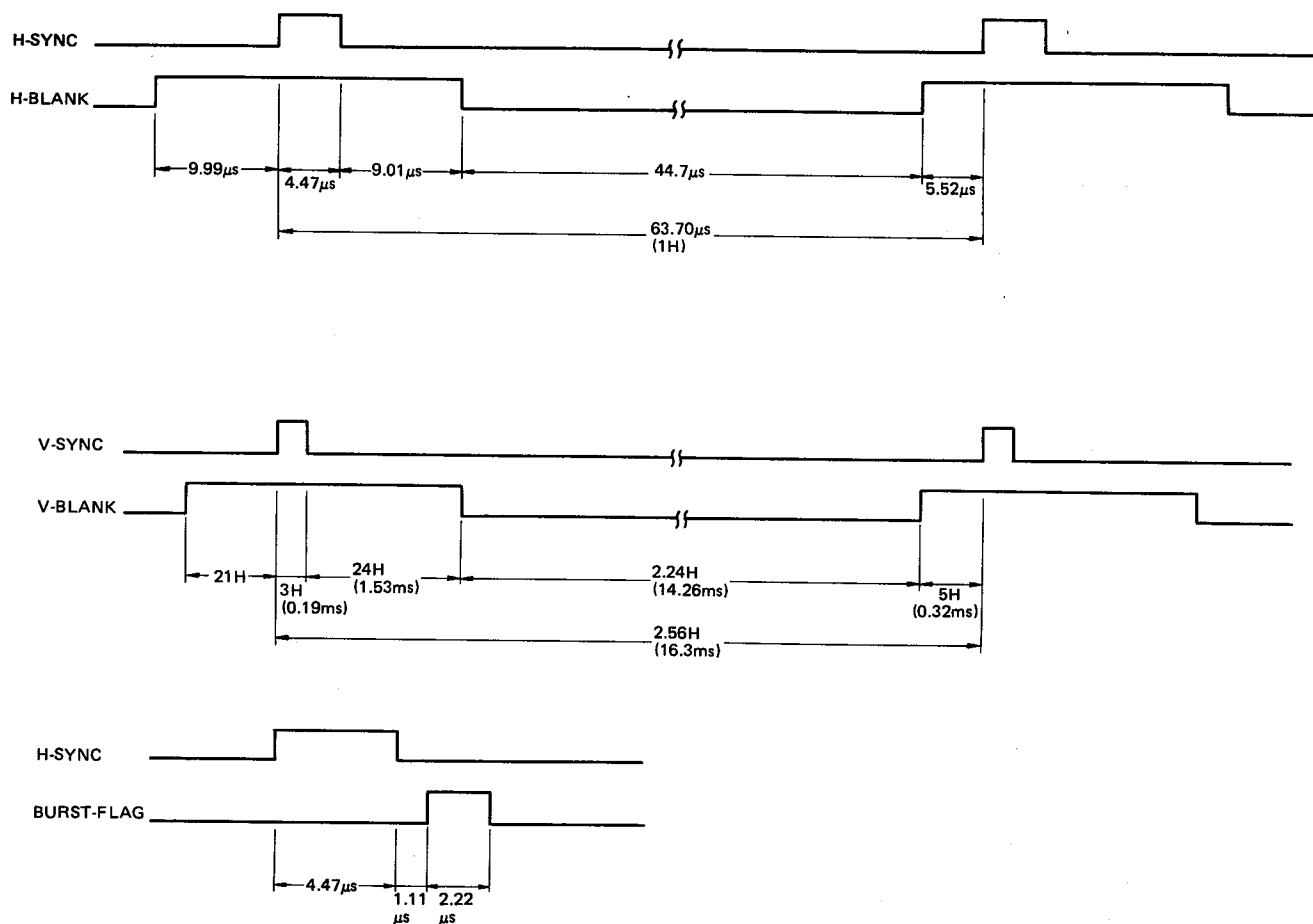
### 7.3. Dynamic RAM R/W Timing

#### (1) Write Timing (All levels are TTL level:5 V)



**(2) Read Timing (All levels are TTL level:5 V)****7.4. CRTC Basic Timing (All levels are TTL level:5 V)**

## 7.5. CRTC Synchronizing Timing (All levels are TTL level:5 V)



## 7.6. Keyboard Scanning

4-bit Data				Key Scan Data (decoded data)									
D	C	B	A	KST0	KST1	KST2	KST3	KST4	KST5	KST6	KST7	KST8	KST9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

## 8. Circuit Descriptions (See the waveforms 7.2.)

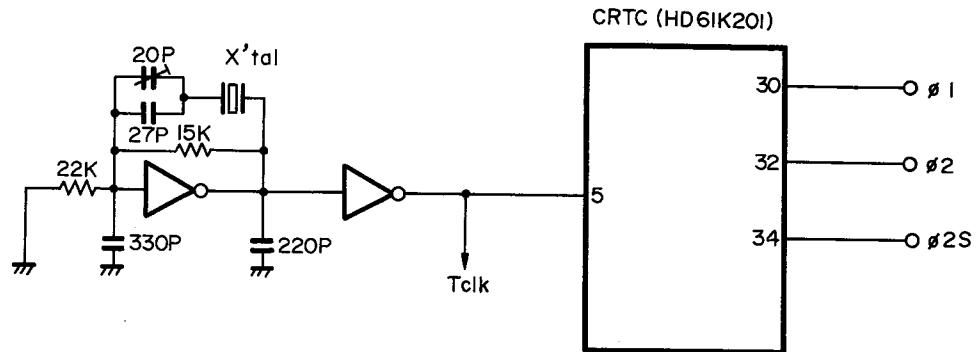
### 8.1. Basic Timing Generator.

Timing for the JR-200U is provided by the basic timing generator composed of a crystal oscillator and CRT controller (CRTC: 80-pin flat package).

TCLK is the crystal oscillator frequency with a middle frequency of 14.31818 MHz (four times the burst frequency in the NTSC system).

$\phi_1$  and  $\phi_2$  are two-phase clocks required by the CPU.  $\phi_2S$  is a clock required by the peripheral LSI. The  $\phi_2$  and  $\phi_2S$  signals are similar, but the latter is required because the phases of  $\phi_1$  and  $\phi_2$  change when reading from or writing into the dynamic RAM. \*1 (Details are described in paragraph 18-3, Dynamic RAM)

\*1 Because hardware timers are operated from  $\phi_2S$  as the standard clock, correct timer values cannot be obtained if the phase of the standard clock changes.



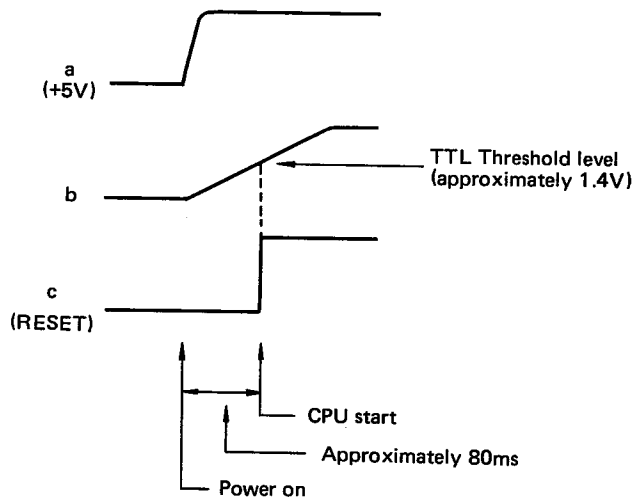
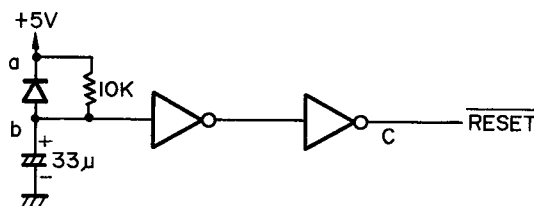
### 8.2. CPU

An MN18A00 (1.5 MHz version) is used as the CPU.

The CPU is synchronized by clocks  $\phi_1$ ,  $\phi_2$ , and  $\phi_2S$  from the basic timing generator. The repetition frequency of  $\phi_2S$  is approximately 1.34 MHz, but its pulse width is approximately 0.28  $\mu s$ , so a 1.5 MHz CPU is used, providing some tolerance.

#### (1) Reset Operation at Power-on

A reset signal is generated to operate the CPU properly from its starting address and initialize the system when power is turned on.



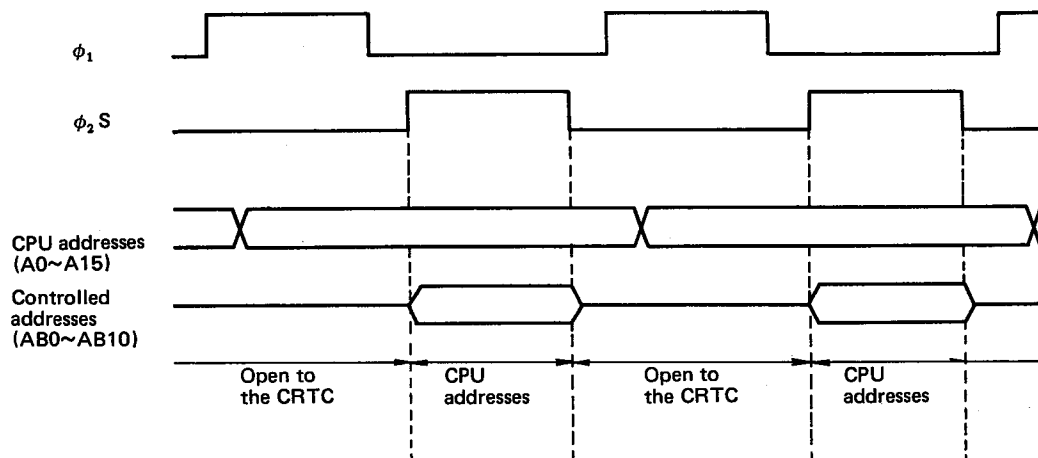


## (2) Address Bus Signal Control

The video refresh memory (VRAM) and character pattern memory (CRAM) are used by the CPU and CRT controller.

In the JR-200U, the CPU and CRT controller time-share the VRAM and CRAM.

CPU address bus signals are output only at  $\phi_2 S$  timing so the address bus must be controlled to open other timing to the CRT controller.



Address bus control timing

As shown in the timing chart, CPU addresses (A0 to A15) are sent to the controlled address bus (AB0 to AB10) at  $\phi_2 S$  periods only, and held in the pending state during other periods.

## (3) Data Bus Signal Control

Like address bus signals, data bus signals are used by the CPU only at  $\phi_2 S$  timing, and those at other times are sent to the CRT controller.

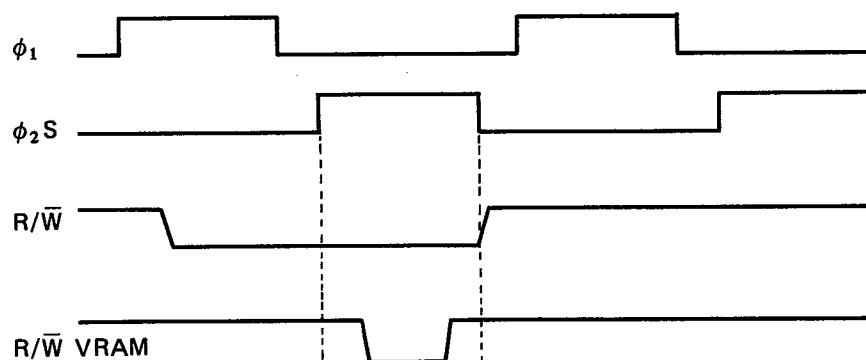
This is done by controlling the bus transceiver (74LS245) with  $\phi_2 S$  and read/write signals.

## (4) Read/write Signal Control

The VRAM and CRAM may use the same device with continuous timing from the CPU and CRT controller.

In this case, CPU read/write signals are input into the VRAM and CRAM after control signals to prevent malfunction at the change of timing while writing from the CPU.

This control circuit is included in the CRTC.



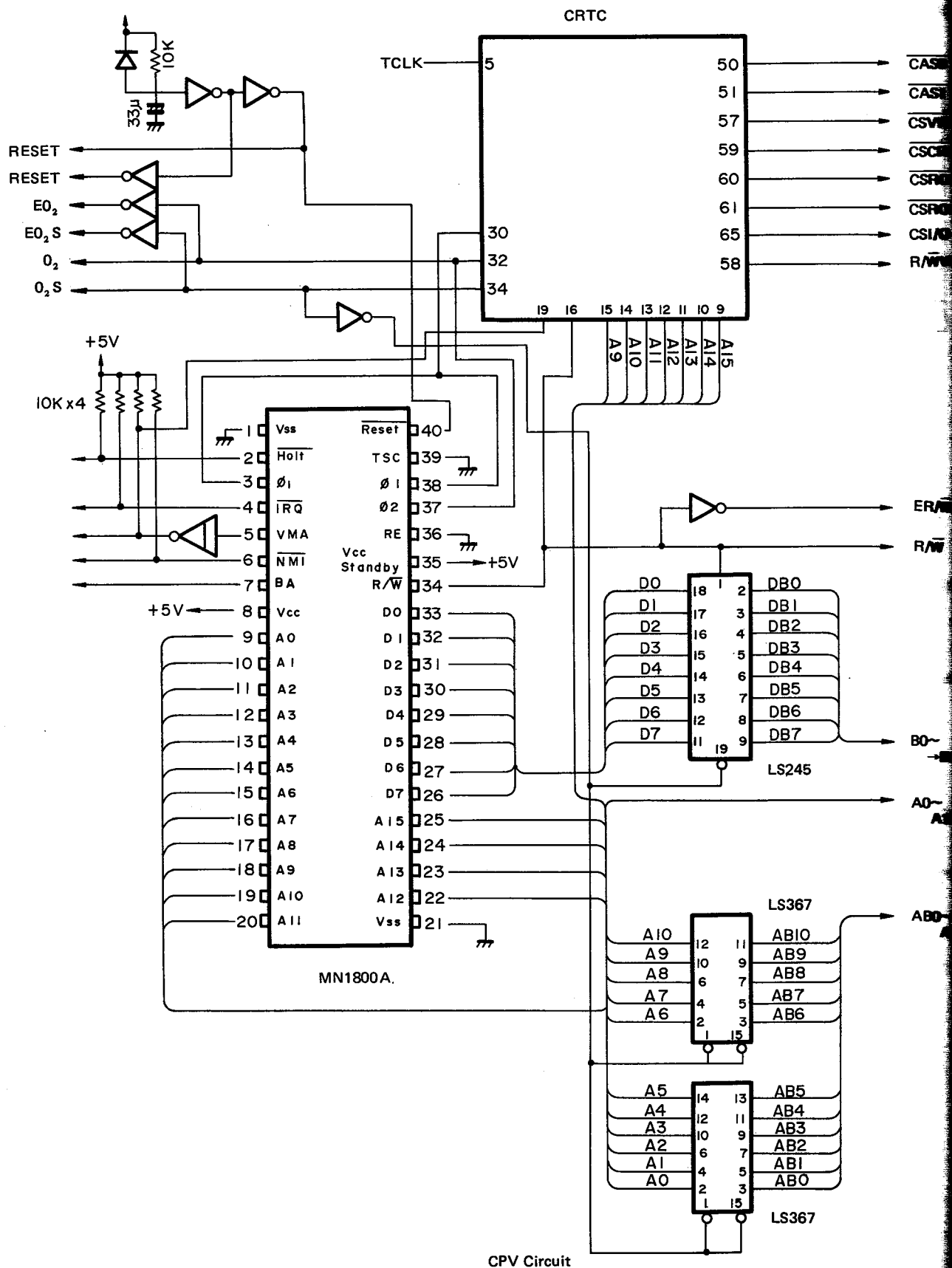
(Note) R/W VRAM — Read/write signals to VRAM and CRAM.

**(5) Device-select Signal Generation**

Device-select signals are generated to select devices allocated on the memory map. In the JR-200U, these signals are included in the CRTC functions to reduce the quantity of elements.

Address signal							VMA	Signal name	Address space	Application
A15	A14	A13	A12	A11	A10	A9				
0	0	*	*	*	*	*	1	CAS0	0~S3FFF	Dynamic RAM
0	1	*	*	*	*	*	1	CAS1	S4000~S7FFF	
1	1	0	0	0	*	*	1	CSV RAM	SC000~SC7FFF	VRAM
1	1	0	1	0	*	*	1	CSCRAM	SD000~SD7FF	CRAM
1	1	0	0	1	0	0	1	CS I/O	SC800~SC9FF	I/O Chip (MN1271)
1	1	0	0	1	1	0	1		SCA00~SCBFF	CRTC

**(Note)** For CSV RAM and CSCRAM, address select signals are output even at the timing used by the CRT controller.



### 8.3. Dynamic RAM

The main storage in the JR-200U uses 64-kilobit dynamic RAMs. They are used to reduce the quantity of elements.

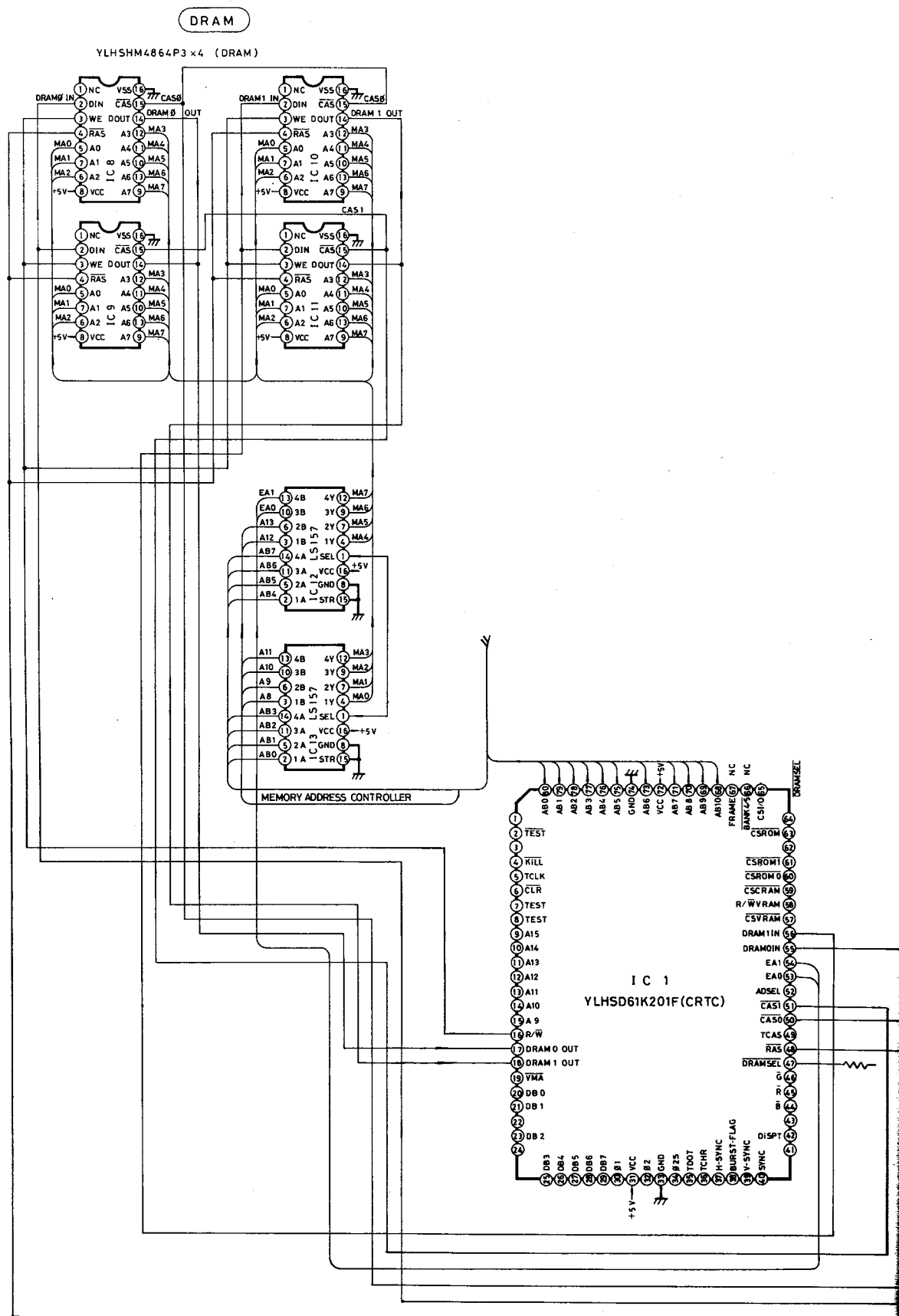
For efficient memory use in byte lengths, parallel-to-series and series-to-parallel conversions are made at write and read respectively using two 64-kilobit dynamic RAMs for a capacity of 16 kilobytes.

#### (1) Write Operation (See the waveforms 7.3(1)).

- W1, W2: Data bus signals are divided into upper and lower segments of 4 bits each, which are latched in two shift registers.
- W3: The lower 8 bits (AB0 to AB7) of an address bus signal are input to the memory address to send RAM signals.
- W4: Address bus signals (A8 to A13) and external addresses (EA0, EA1) are input to the memory address, and the shift register lower bits are written upon input of CAS signals.
- W5: The external address is advanced by one and the shift register is shifted by a bit.
- W6: The same operation as W4 is performed.
- W7: The same operation as W5 is performed.
- W8: The same operation as W4 is performed.
- W9: The same operation as W5 is performed.
- W10: The same operation as W4 is performed.
- W11: The write operation is complete.

#### (2) Read Operation

- R1: The lower 8 bits of address bus signals are input to the memory address to send RAS signals.
- R2: Address bus signals (A8 to A13) and external addresses (EA0, EA1) are input to the memory address, and CAS signals are input to store the output data of the memory in the shift registers.
- R3: The external address is advanced by one and the shift register is shifted by a bit.
- R4: The same operation as R2 is performed.
- R5: The same operation as R3 is performed.
- R6: The same operation as R2 is performed.
- R7: The same operation as R3 is performed.
- R8: The same operation as R2 is performed.
- R9: The contents of the shift registers are arranged in the same two 4-bit groups as those latched at the time of a write operation, and the 4 bits from each of the two registers are output to the data bus.
- R10: The read operation is complete.

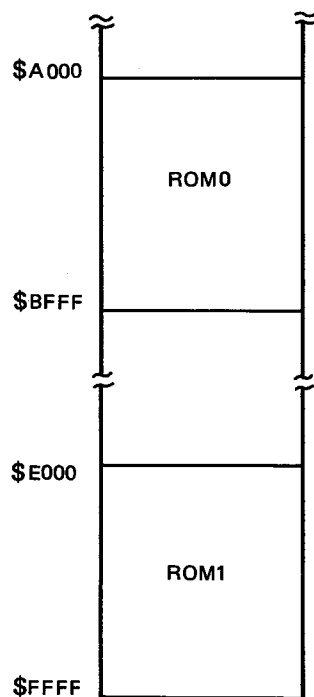


## 8.4. ROM

The ROM has a capacity of 16 kilobytes, being composed of two 8-kilobyte mask ROMs.

A BASIC interpreter and an I/O control routine are included in the ROM.

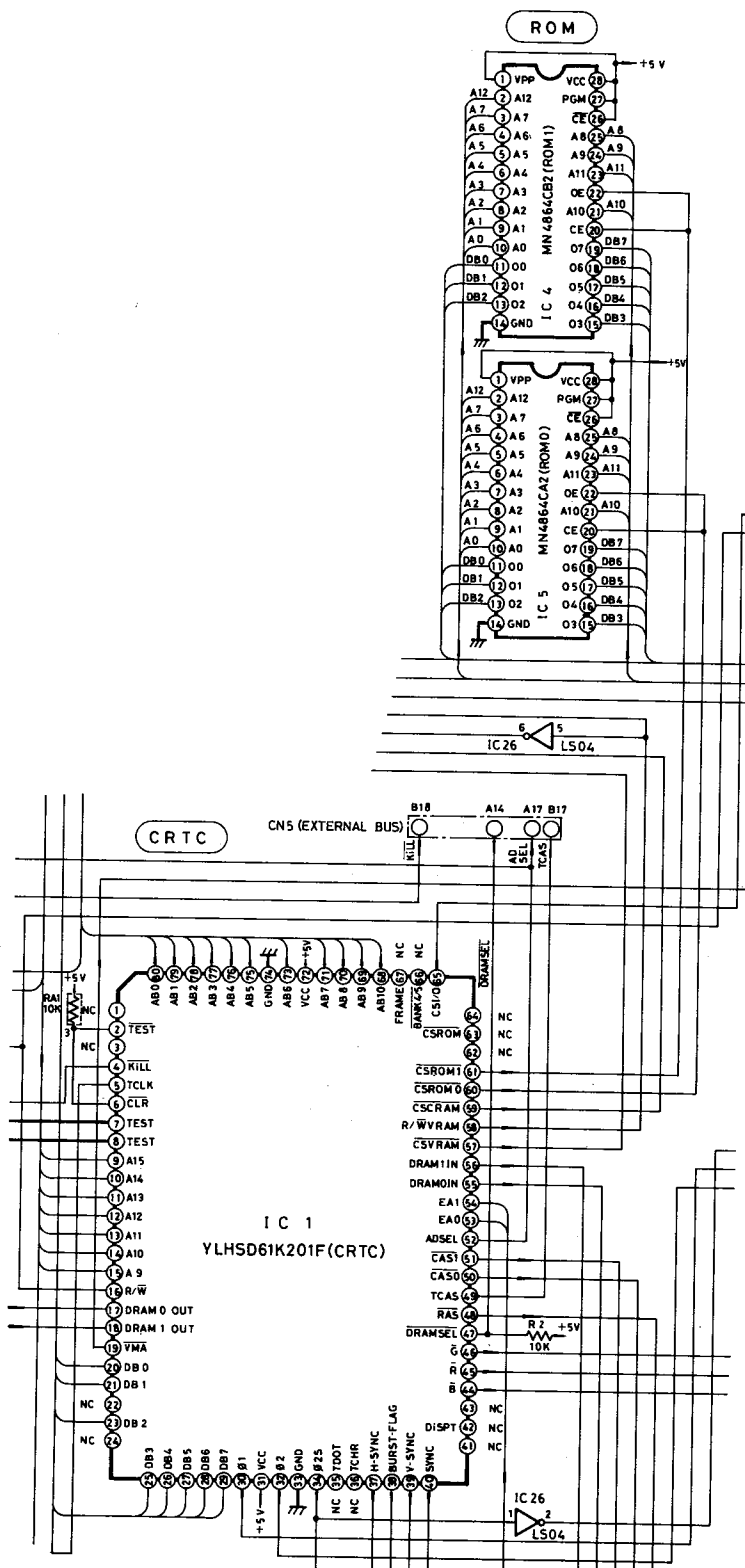
[ROM Memory Map]



Chip select signals for ROM0 and ROM1 are output to the ROM from the CRTC. The CRTC also controls the ROM as follows:

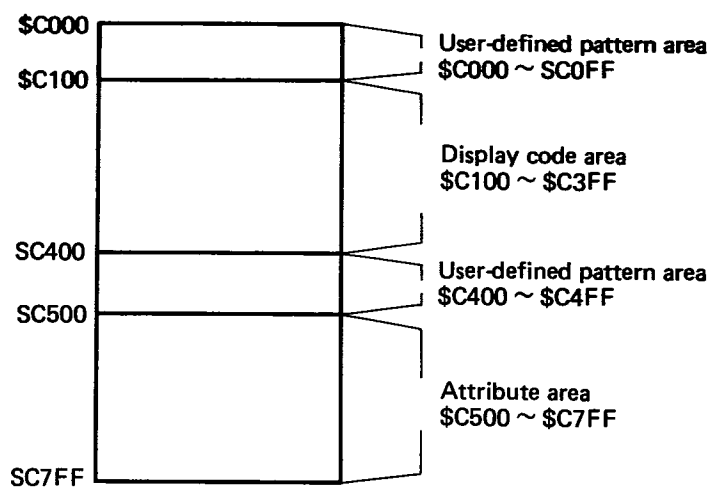
[KILL signal]

When the four-pin (KILL) input to the CRTC is at ground level, a chip select signal (CSROM0) for ROM0 is not output even if the CPU accesses addresses \$A000 to \$BFFF. ROM0 includes a BASIC interpreter, which can override calls to ROM0 as when floppy disk BASIC is used.



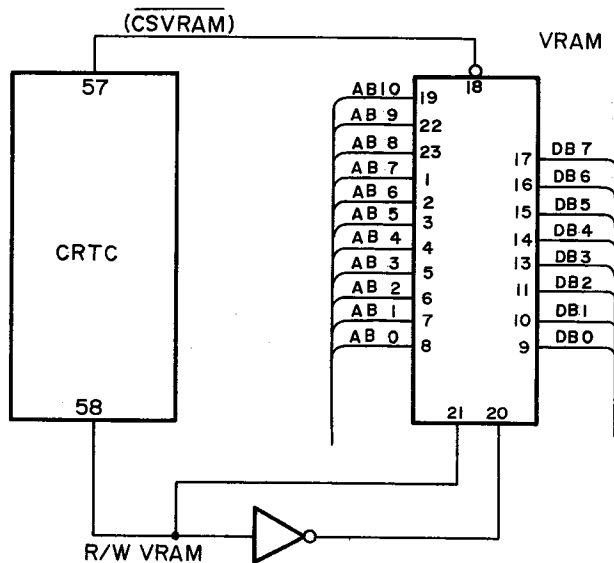
## 8.5. Video Refresh RAM

The VRAM employs a 2-kilobyte static RAM.



VRAM Memory Map

The VRAM is divided into four areas, as shown in the memory map. Details are described in the CRT controller paragraph.



The chip select signal (CSV RAM) and read/write signal (R/W VRAM) for the VRAM are output from the CRTC.



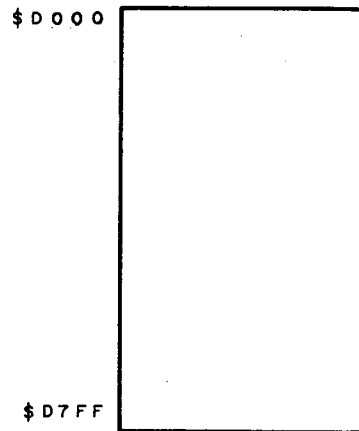
## 8.6. Character Generator RAM

The CRAM employs a 2-kilobyte static RAM.

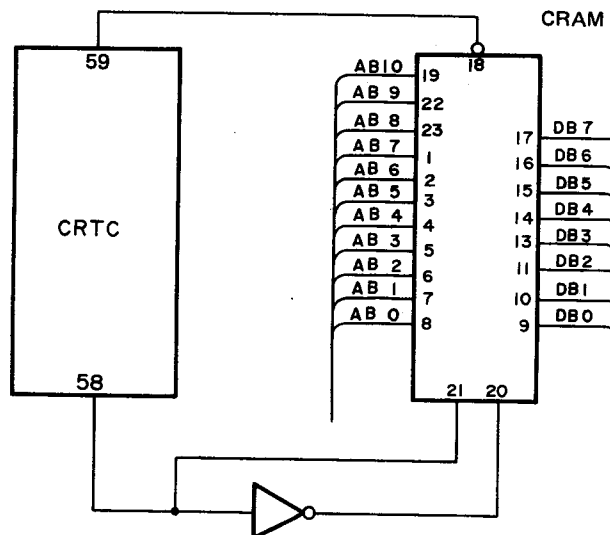
A ROM is usually used for this function, but the JR-200U uses a RAM because it provides faster access.

When power is turned on the CPU through the I/O interface, reads the character patterns contained in the internal ROM of the sub-CPU (MN1544 CJR) and stores them in the CRAM.

[CRAM Memory Map]



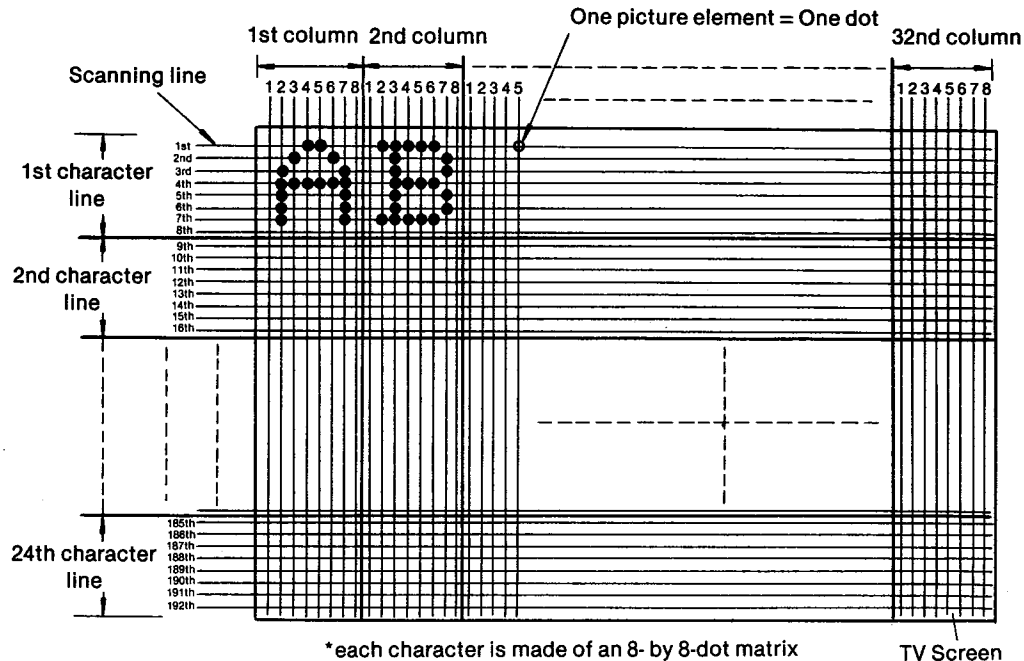
The chip select signal (CSVAM) and read/write signal (R/W VRAM) for the CRAM are output from the CTRC.



## 8.7. CRT Controller and Video Interface

### (1) Basic Operations of the CRT Controller

#### a. Screen formation



Screen Formation

The screen of the JR-200U shown in the figure is formed by:

Character formation	8 x 8 dots
Number of characters	32 characters (per line)
	x 24 lines

The CRT displays 32 characters per line, using eight horizontal lines. The effective 256 (8x32) dots in a horizontal line are controlled by the dot clock ( $T_{dot} = 7.15909 \text{ MHz}$ ), and character timing (TCHR) is generated every eight dots to control the characters. The lines are controlled by the counter that counts every eight horizontal lines.

#### b. Display character and character pattern control

The controller has two kinds of information, character information and color information (attribute), in the video refresh memory (VRAM), and character pattern information in the character pattern memory (CRAM), displaying color-controlled characters on the CRT. Memory addresses in the display code area of the VRAM are allocated corresponding to display positions on the screen.

(column)

	0	1		31
0	\$C100	\$C101		\$C11F
1	\$C120	\$C121		\$C13F
23	\$C3E1	\$C3E1		\$C3FF

(line)

[Display Position on Screen and Display Code Area of VRAM]

The data in this area is a character code used in BASIC in the normal display mode (normal mode).

Color information is stored in the attribute area. Memory addresses in this attribute area, like those in the display code area, are allocated corresponding to display positions on the screen.

The data in address \$C100 in the display code area is displayed on the screen according to that of address \$C500.

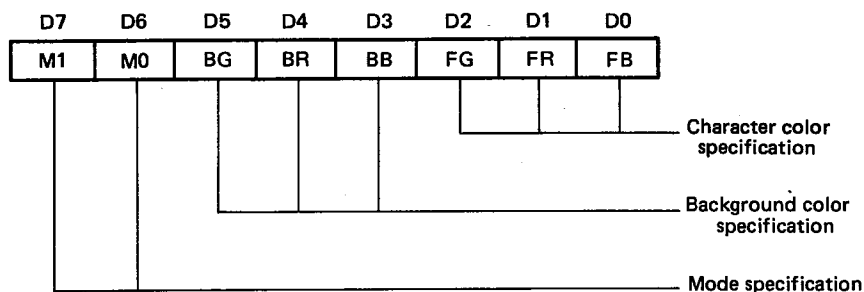
(column)

	0	1		31
0	\$C500	\$C501		\$C51F
1	\$C520	\$C521		\$C53F
23	\$C7E0	\$C7E1		\$C7FF

(line)

[Display Position on Screen and Attribute Area of VRAM]

- Contents of Attribute



- Color Specification

	G	R	B
Black	0	0	0
Blue	0	0	1
Red	0	1	0
Violet	0	1	1
Green	1	0	0
Light blue	1	0	1
Yellow	1	1	0
White	1	1	1

- Mode Specification

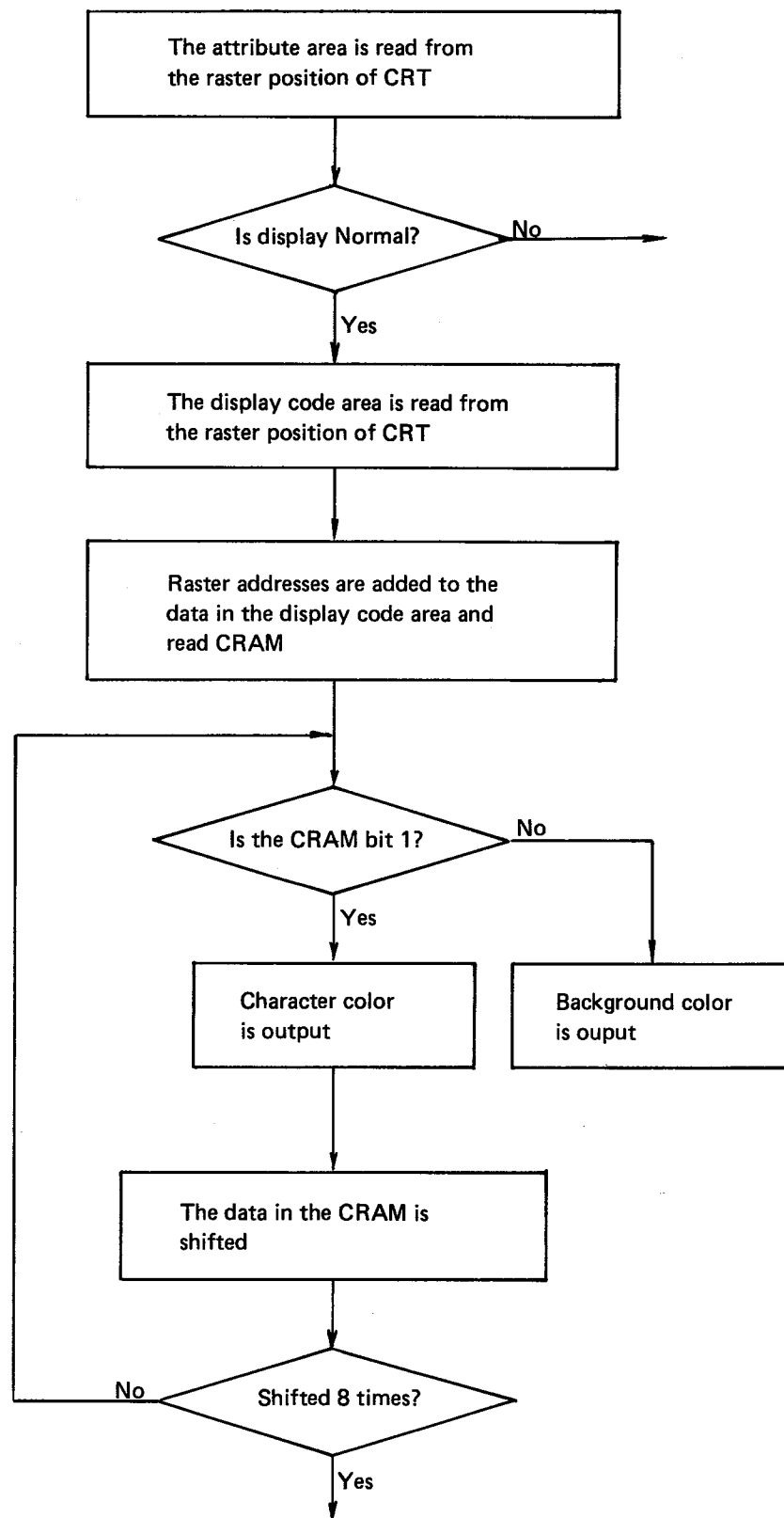
M1	M0	Mode
0	0	Normal display mode
0	1	User-defined display mode
1	0	Semi-graphic display mode

(Note) Inverted display is performed, exchanging character color specification with background color specification, by software.

If the mode in the attribute area corresponding to the display position on the screen is specified as the normal mode, the CRAM data is read out because display patterns are obtained from the display code area. (The data in the display code area and those indicating the positions of eight horizontal lines are read out as the addresses of the CRAM.)

The CRAM pattern data, CRAM, attribute character color information if the CRAM bit is 1 and background color information if 0, are output to the CRT while being shifted in bits by the dot timing.

[Character Display Flow in Normal Display Mode]



c. **User-defined pattern display [M1=0, M0=1]**

If the attribute area mode is specified as user-defined pattern display mode, character patterns are determined by the data in the user-defined pattern area and not by those in the CRAM.

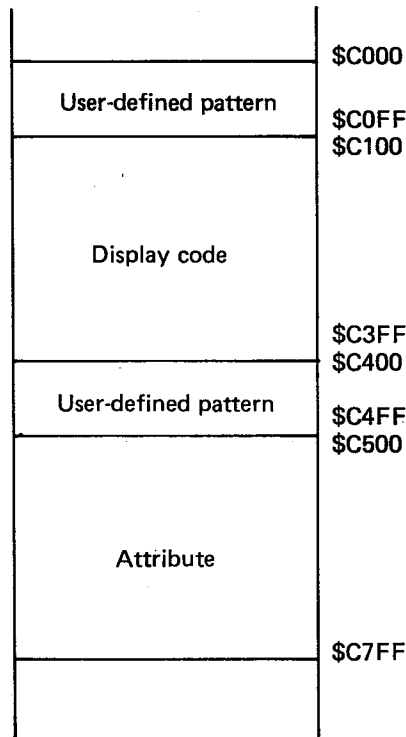
The JR-200U allows 64 user-defined patterns.

Character codes that can be defined by users

\$20 (Space) ~ \$3F (?) [\$C000 ~ \$C0FF]

\$40 ( @ ) ~ \$5F (—) [\$C400 ~ \$C4FF]

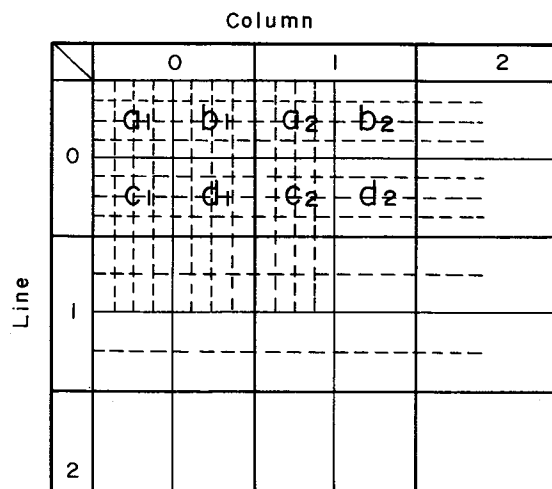
● User-defined pattern area



d. **Semi-graphic display [M1=1, M0=0]**

If the attribute area mode is specified as the semi-graphic display mode, character patterns are not displayed, but the four quarters of each 8x8-dot area are specified as a color and displayed according to the data in the display code area and attribute area. Each quarter is formed of 4x4 dots, and is specified in color as follows:

[Display Position on Screen]



[Contents of VRAM Semi-graphic Display]

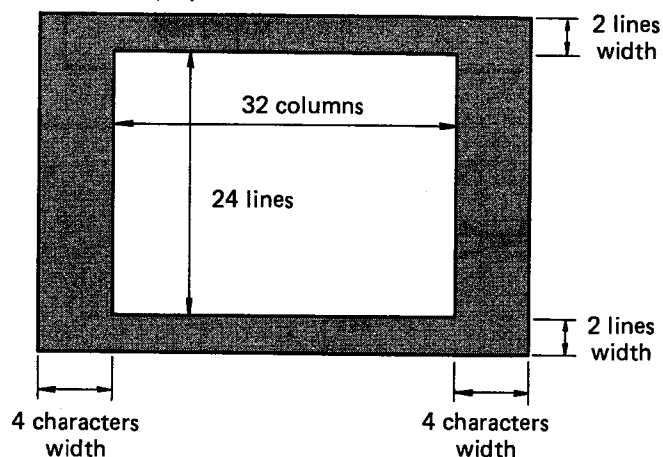
	D7	D6	D5	D4	D3	D2	D1	D0
\$C100			G	R	B	G	R	B
			b1			a1		
\$C101			G	R	B	G	R	B
			b2			a2		
\$C500	I	O	G	R	B	G	R	B
			d1			c1		
\$C501	I	O	G	R	B	G	R	B
			d2			c2		

e. Frame display

The CRT controller of the JR-200U provides for frame display.

The frame is a mono-color display around the effective screen area of 32 characters x 24 lines.

[Frame Display]



The frame is composed of a four-character space on each side and a two-line space on each end.

The frame color is displayed as the color specified by writing color data in address \$CA00.

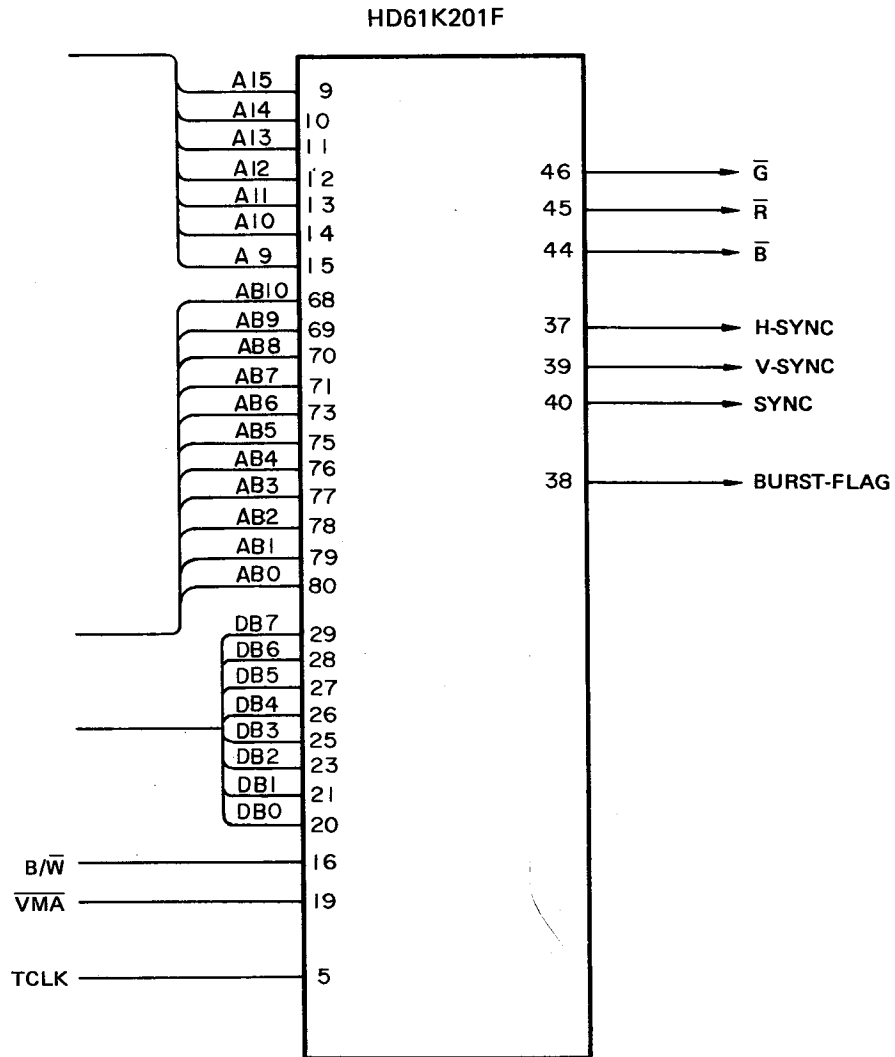
Data	Color
0	Black
1	Blue
2	Red
3	Violet
4	Green
5	Light Blue
6	Yellow
7	White

The low-order three bits of the data written in address \$CA00 are valid, but the upper bits are ignored.

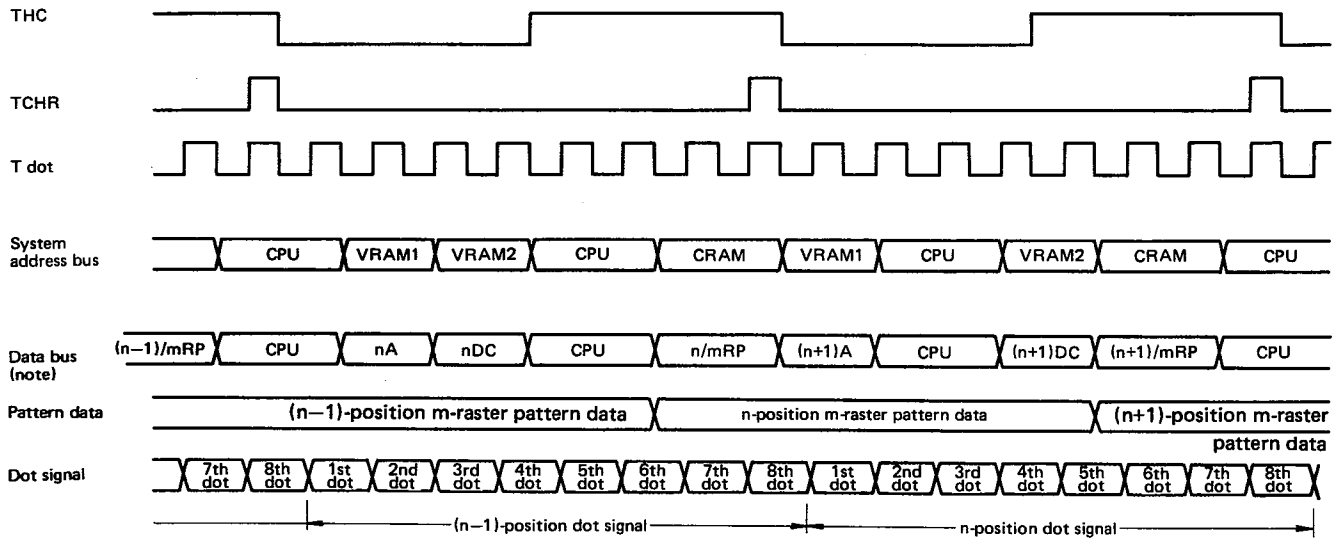
Only writing to this address is valid; reading is impossible.

## (2) Video Signal Generator

The CRTC (CRT controller) of the JR-200U is composed of an exclusive LSI shown in the circuit diagram.







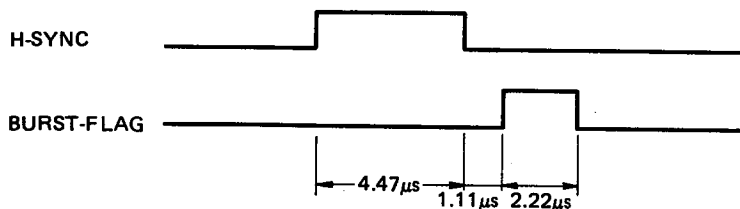
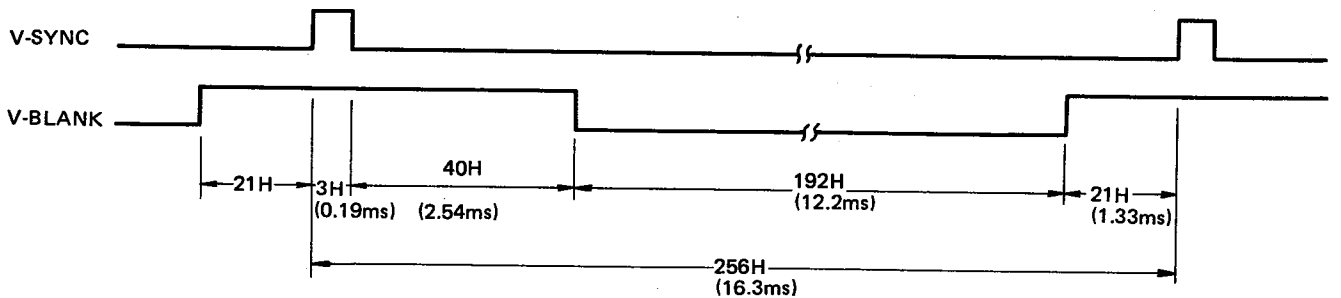
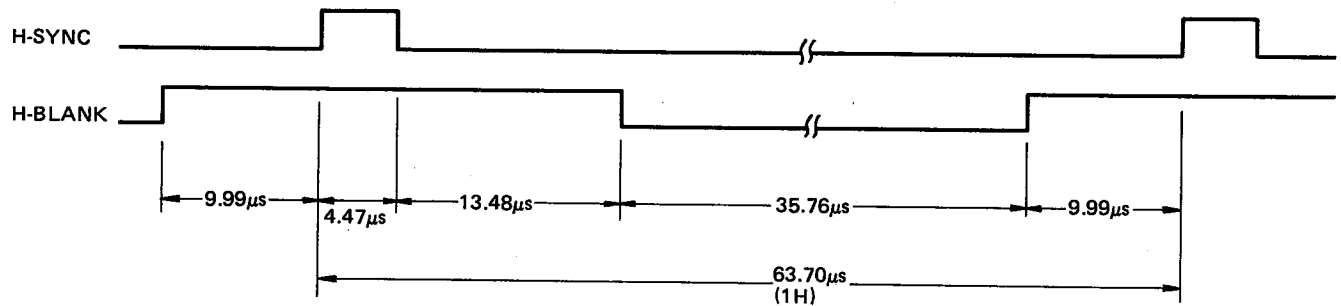
(Note)

1. (n-1)/mRP means (n-1)-position m-raster pattern data

2. nA means n attribute

3. nDC means n display code

[CRTC Basic Timing Chart]



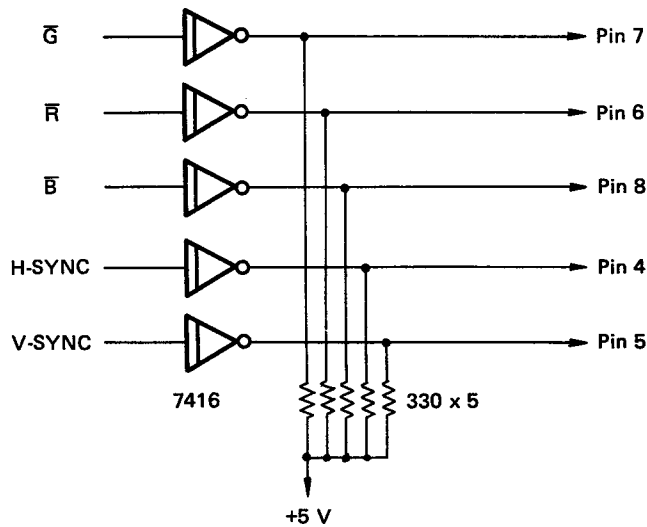
[CRTC Synchronizing Timing Chart]

### (3) Video Signal Processor

The JR-200U has three kinds of video outputs.

a. RGB synchronizing signal separation output

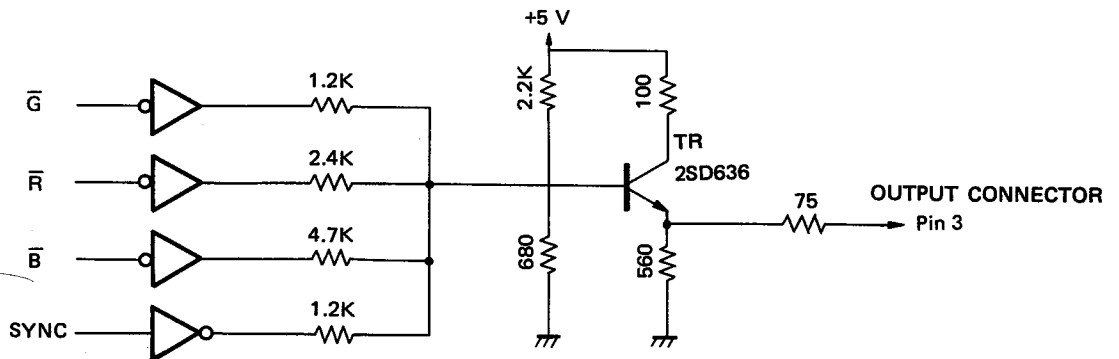
This video signal is output to the connector through a buffer because the CRTC needs output circuit, buffering.



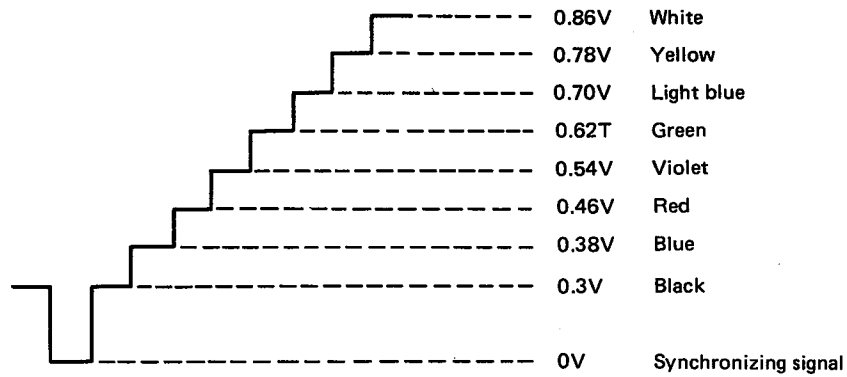
b. Composite video signal output

Because composite video signals are not generated in the CRTC, an external circuit is added to generate the signals.

Luminance signals are generated by the resistance adder from R.G.B. signals and synchronizing signals.



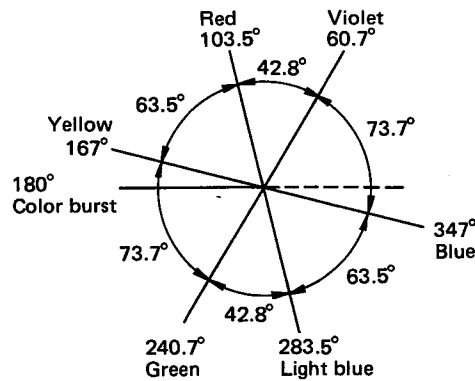
Luminance signals are selected so that signal R is 2 and signal G is 4 when the deviation of signal B is 1.



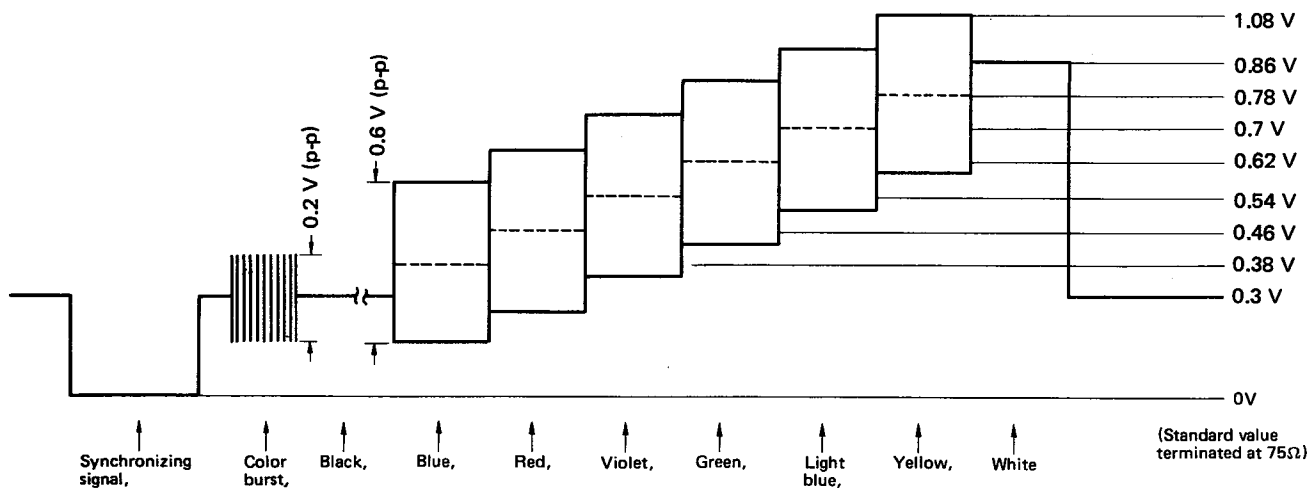
(Note) Voltage terminated in 75Ω.

### Color signal formation

Color signals for the eight colors should be added to the luminance signals as a phase difference to the burst signal (3.579545 MHz).

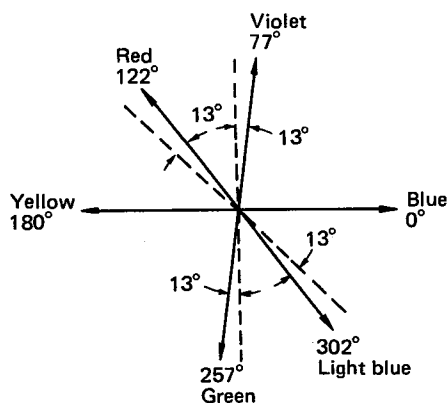


[Phase of Color Signal in NTSC System]



[Color Composite Video Signal]

The phase difference can be considered below, based on the timing chart.



When the TTL gate delay is 10 ns (TPY), a phase difference of approximately 13 degrees occurs at  $f_0=3.579545$  MHz. The counter output is used as a color signal in the NTSC system, making use of that phase difference.

The color signal selected by R.G.B. signals is added to the luminance signal by the resistance adder through the filter.

Also the burst signal, like the color signal, is added to the luminance signal by the resistance adder through the filter after BURST and AND output from the CRTC are provided. The burst signal phase-adjusts the filter circuit for the phases of color and burst signals.

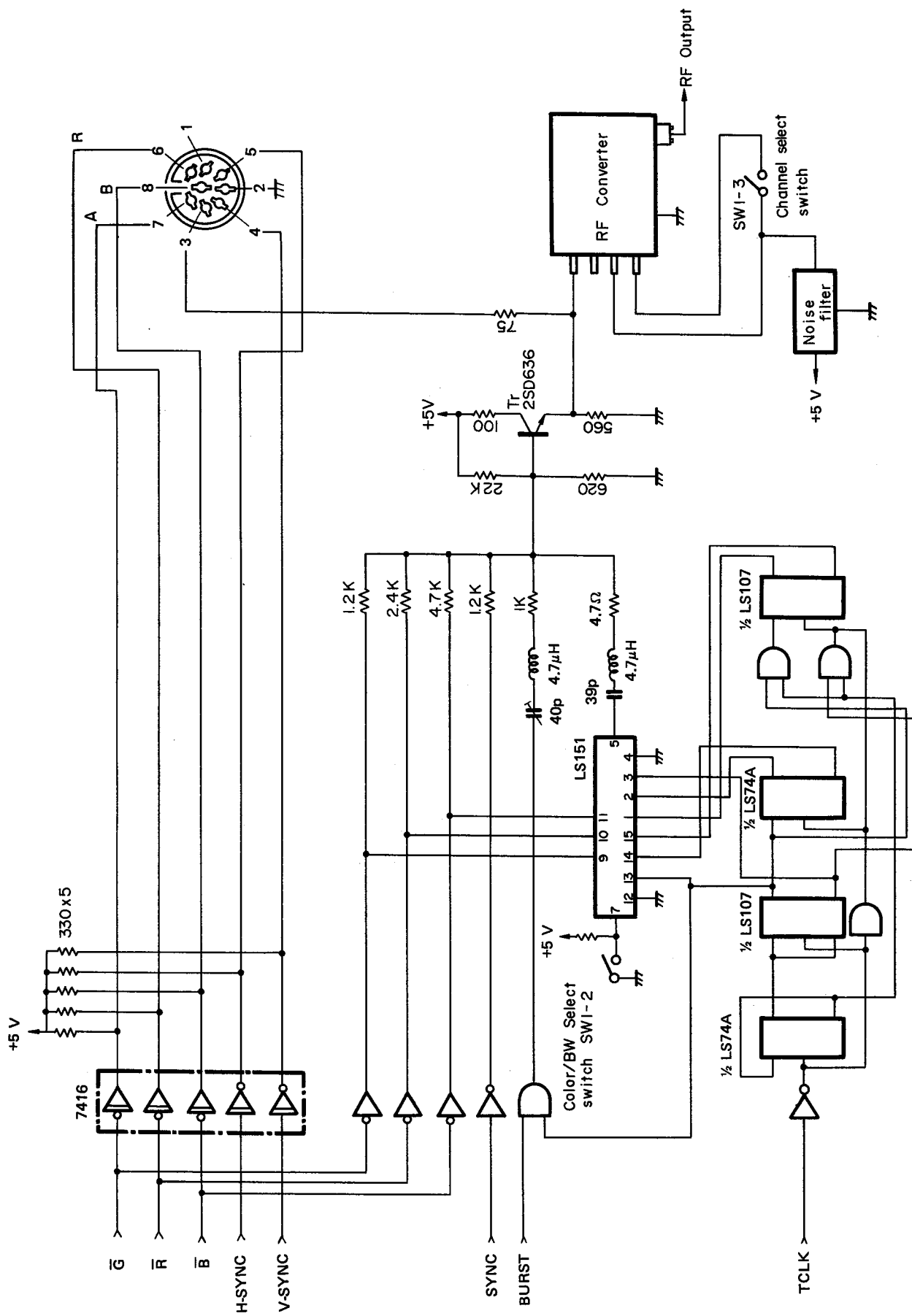
When a black-and-white monitor is used, the display quality is degraded if the color signal is added. To avoid this, a switch (SW1-2) is provided to cut the color signal.

The composite signal made in the resistance adder is output to pin 3 of the connector through the emitter follower circuit and the 75-ohm series resistance.

c. RF signal

Composite video signals are output to a pin jack after modulation by the RF converter to connect the JR-200U to a home television.

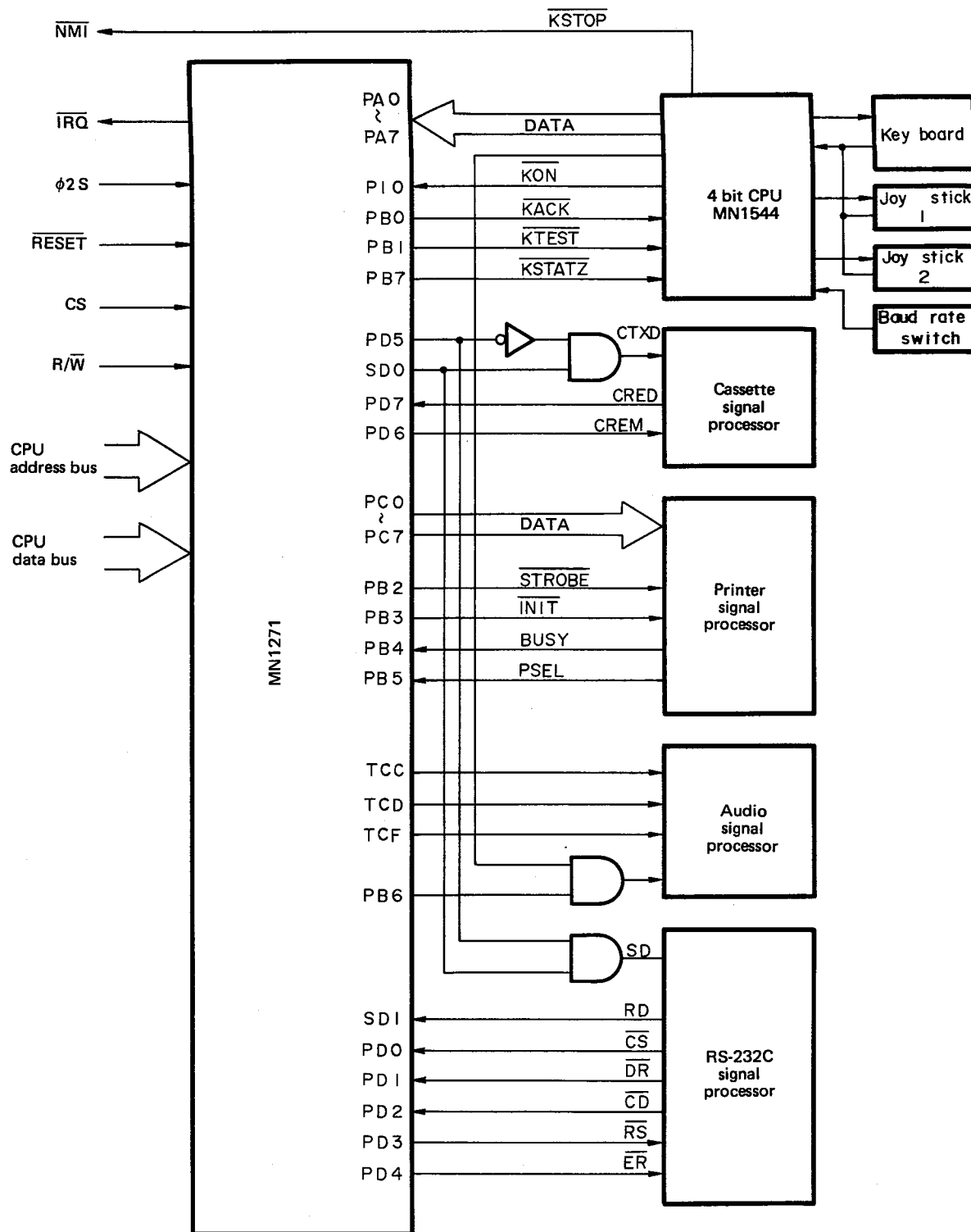
Channel 3 or 4 of the television is chosen with the DIP switch (SW1-3).

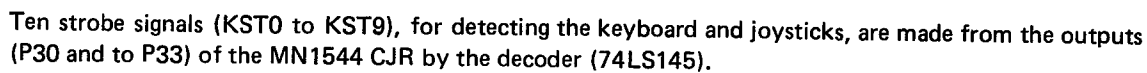


**[Video Interface Circuit]**

## 8.8. I/O Interface (PIA)

The I/O interface is composed of the MN1271 and other hardware.





a. Keyboard interface functions

- Transfer of display character patterns

Transfers character patterns stored in the MN1544 when initiated by KTEST signals just after power is turned on.

- Transfer of baud rate information

Transfers baud rate information after transferring character patterns, when initiated by KTEST signals just after power is turned on.

- Transfer of key information

Transfers character codes assigned to keys when keys are depressed.

- Transfer of joystick information

Transfers joystick 1 and 2 information (each 1 byte of ON/OFF data) together with character codes.

b. Interface signal functions

- KSTOP signal (BREAK key detection and interrupt signal) KSTOP is an output pulse indicating that the BREAK key is depressed. This signal is connected to the CPU non-maskable interrupt (MNI) input.

- KON signal (ON key interrupt signal)

KON is an output pulse indicating that the 4-bit CPU requires the main CPU to transfer data.

This signal is connected to P10 of the MN1271. When the signal is output, the data to be transferred is set up.

- KDATA signal (Data signal)

KDATA is a data signal sent by the 4-bit CPU.

- KSTAT2 signal (Operation mode control status signal)

KSTAT2 is used to specify the input information transfer system (\*1) to the 4-bit CPU.

- KACK signal (Data read complete response signal)

KACK is a response signal (pulse signal) indicating that the main CPU has received KON signals and read KDATA signals.

- KTEST signal (Key test signal)

KTEST is a signal indicating that the main CPU requires the key test result.

Processing by 4-bit CPU

a) Key buffer data not yet sent or now being sent are all made invalid.

b) Key and joystick information is detected and the results are transferred.

c. Input information transfer system

The system defines the operation mode, based on which the 4-bit CPU conducts a keyboard test, by operation mode control status signals (KSTAT2). The operation mode may be BASIC mode or neutral mode. Operation mode is set by keying **CTRL** + **Letter**.

a) KSTAT2 = 0 (BASIC mode)

When **CTRL** + **Letter** is keyed in, letters or the letter code assigned to one letter key is generated.

(Example) When keys **CTRL** + **P** are depressed, the five-letter character code PRINT is generated.

b) KSTAT2 = 1 (Neutral mode)

When **Letter** is keyed in, the transmission code (\$10 to \$18) assigned to one letter key is generated.

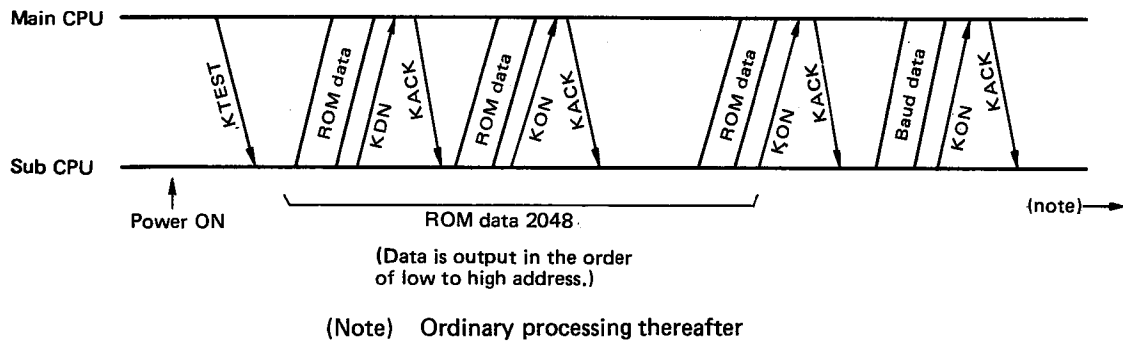
(Example) When key **P** is depressed, character code \$10 is generated.

In this mode, the key operation is valid with letter/numeral mode and graphics mode.

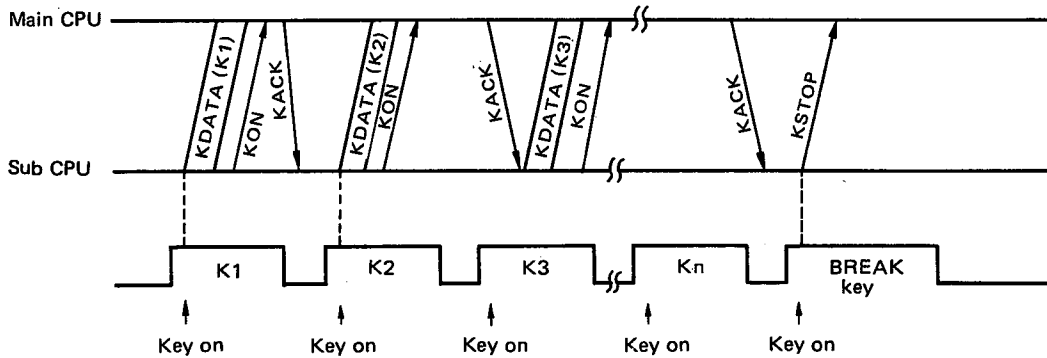


d. Typical procedure

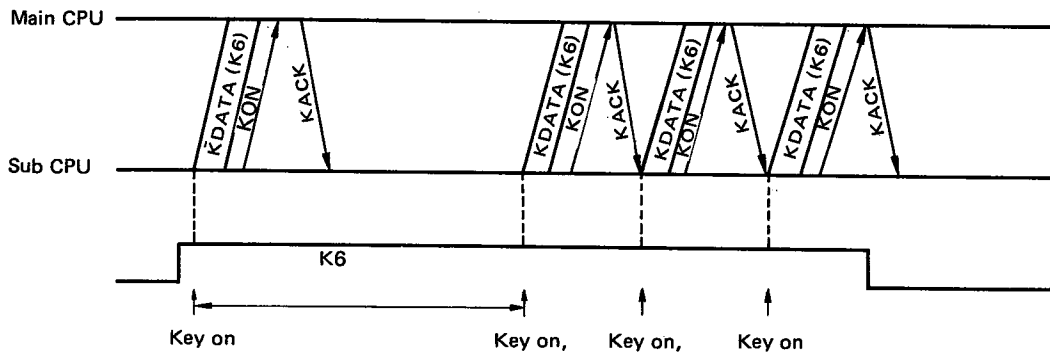
- Immediately after power is turned on.



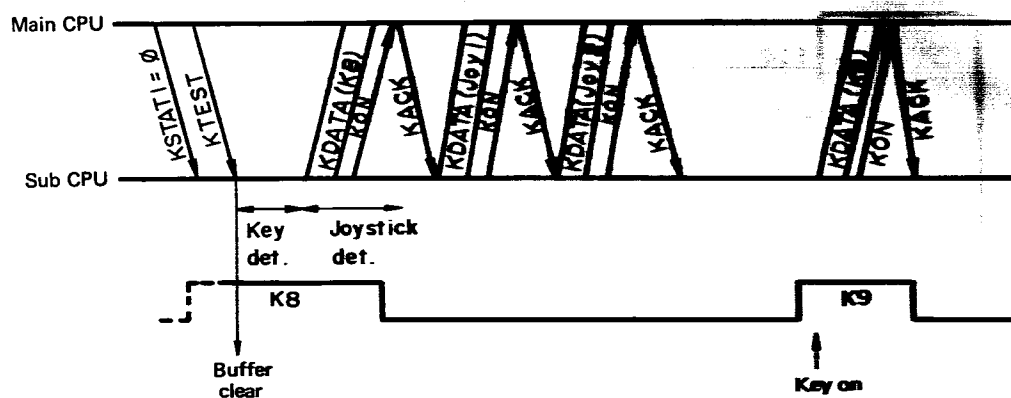
- Ordinary key detection



- Repeat operation



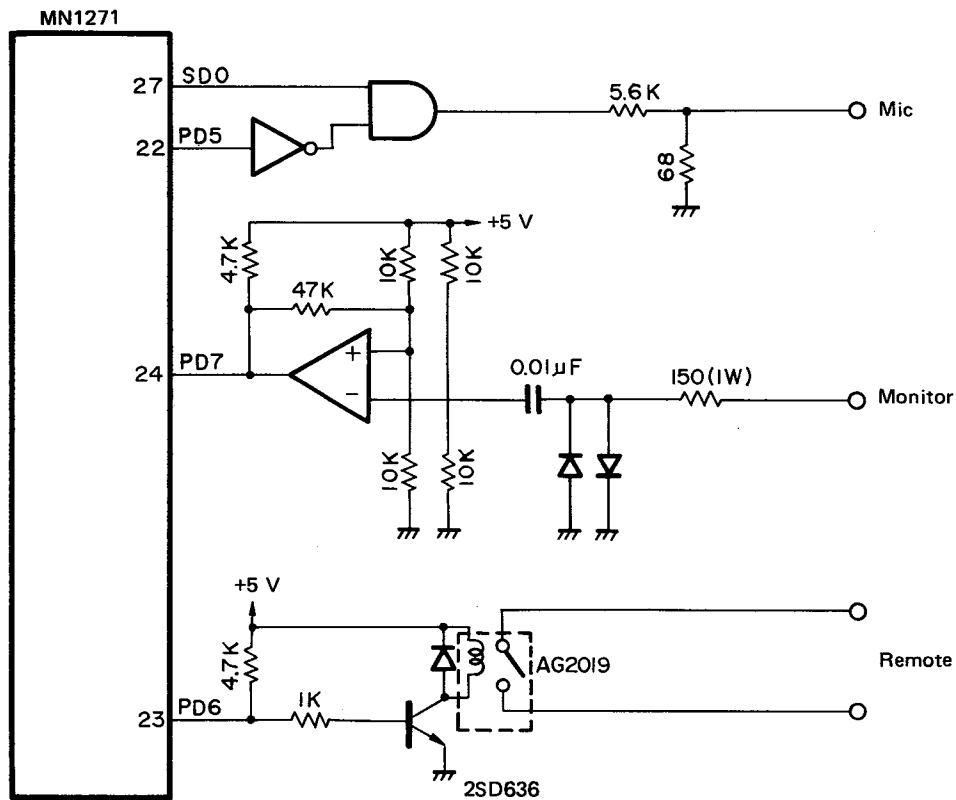
• Key detection required by main CPU



e. Keyboard Matrix

	KST0 (P20)	KST1 (P21)	KST2 (P22)	KST3 (P23)	KST4 (P30)	KST5 (P31)	KST6 (P32)	KST7 (P33)
KIN7 (P53)	2	4	6	8	0	¥		SHIFT
KIN6 (P52)	W	R	Y	I	P	^	DEL	SPACE
KIN5 (P51)	S	F	H	K	;	[	→	GRAPH
KIN4 (P50)	X	V	N	,	/	]	↑	
KIN3 (P43)	Z	C	B	M	.	□	↓	
KIN2 (P42)	A	D	G	J	L	:	←	RETURN
KIN1 (P41)	Q	E	T	U	O	@	INS	RUBOUT
KIN0 (P40)	1	3	5	7	9	-	STOP	CTRL

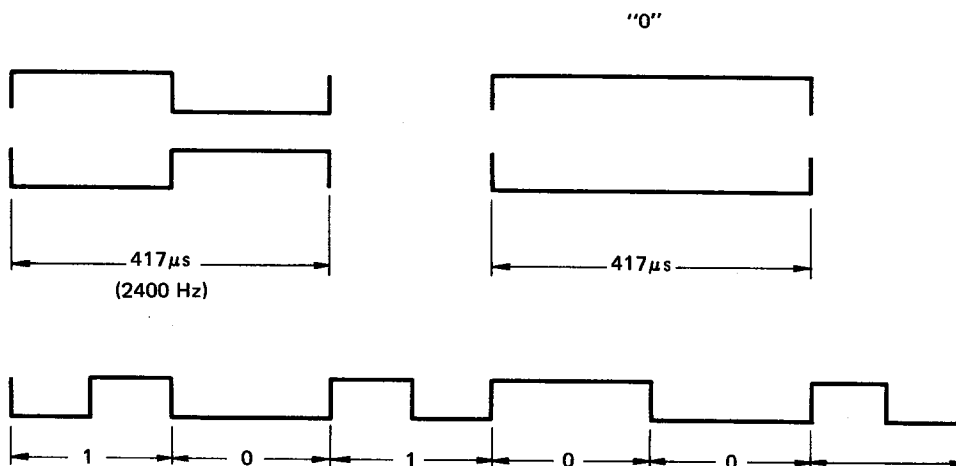
## (2) Cassette interface



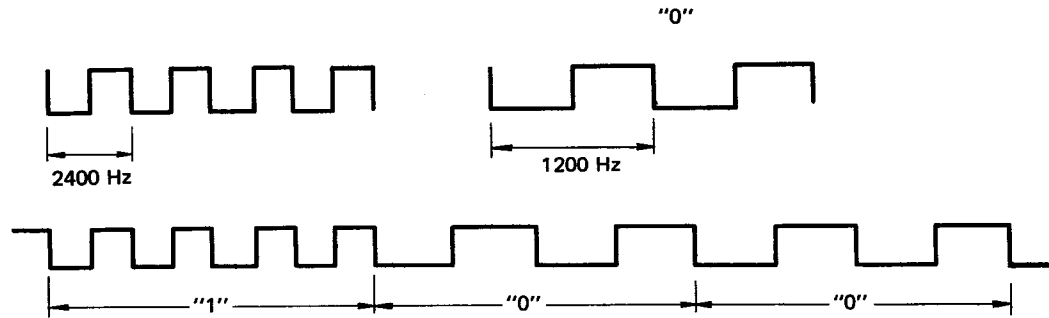
Remote control is possible from the cassette interface. One of the two baud rates, 2,400 and 600 baud, can be selected with the DIP switch on the bottom of the unit.

[Write Waveform]

2400 Baud "1"



600 Baud



#### Writing to cassette tape

Because the write signal is common to the transmitting data signal for the RS-232C, it is controlled by PD5. The write signal is output to the cassette tape when PD5=0.

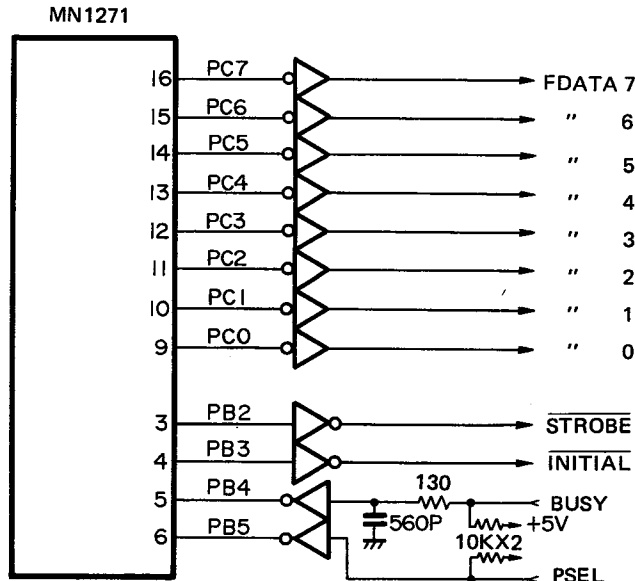
Write signal level: approximately 50 mV (p-p)

#### Reading from cassette tape

The audio output of the cassette tape is input to the comparator (AN6914) through an attenuator.

The comparator has a hysteresis of approximately 0.22 V and converts the input signal to an ON/OFF signal (5 V/ground).

### (3) Printer interface



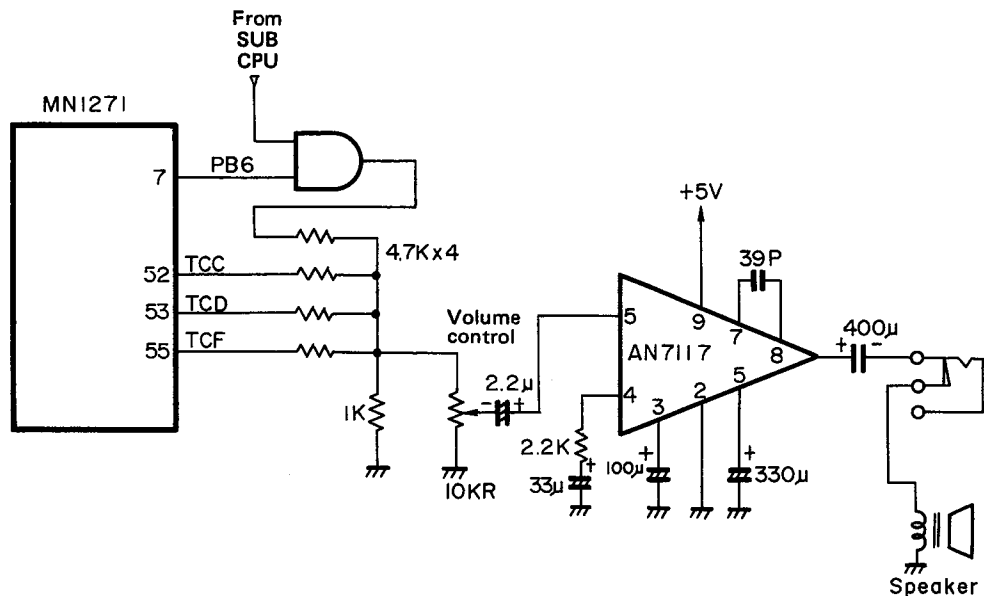
The printer interface is a Centronics-compatible parallel interface.

The following two printers can be used as standard.

JR-P02U	Panasonic	(PSEL=0)
MX-80	Epson	(PSEL=1)

The printer control signals are output from the MN1271 to the connector through the buffer (74LS04) circuit. The input signals from the printer is connected to the MN1271 through the buffer (74LS04).

Refer to the specification manual for each printer for the control sequence.

**(4) Audio interface**

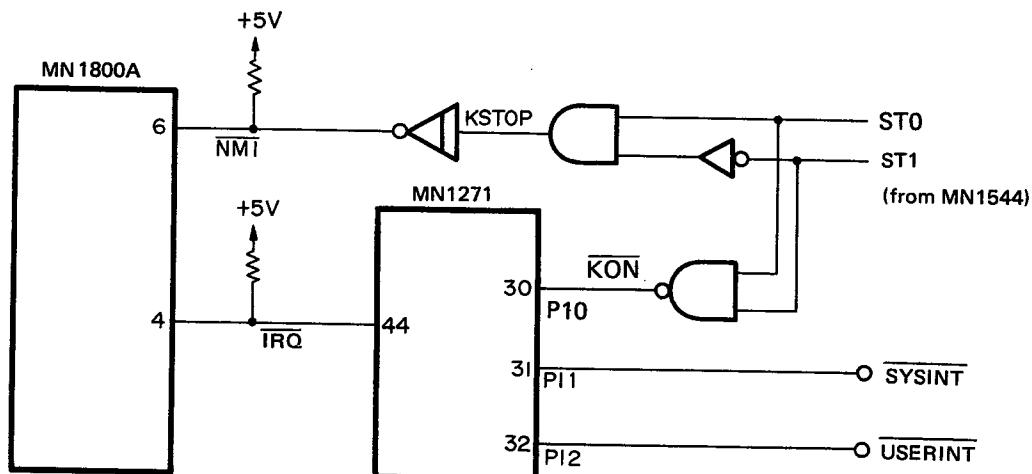
The audio interface mixes three counter (C, D, F) outputs and key detection sounds and amplifies them through the AN7117, driving a speaker.

Key detection sounds can be switched by PB6.

- PB6 = 0 — No key detection sound is generated.
- PB6 = 1 — Key detection sound is generated.

The volume provided for input to the amplifier enables it to drive the speaker at an adequate sound level.

The amplifier output is connected to the external speaker terminal, so an external speaker can be connected. In this case, the internal speaker is cut off.

**8.9. Interrupt Control**

The interrupt control uses the interrupt control functions of the I/O interface and MN1271.

The CPU (MN1800A) has the following two interrupt control signals:

- a. **Non-maskable interrupt ( $\overline{\text{NMI}}$ )**  
A non-maskable interrupt sequence is generated in the CPU automatically at the leading-edge input of NMI signals.

b. **Interrupt request ( $\overline{IRQ}$ )**

This signal is an input for interrupt request. The interrupt sequence is executed in the CPU if the signal is input.

When  $\overline{NMI}$  and  $\overline{IRQ}$  signals are received, the index register, program counter, accumulator, and condition register are stored in stacks and branched to the memory addresses of which contents are shown by the following memory addresses.

$\overline{NMI}$	\$FFFC (Upper address), \$FFFD (Lower address)
$\overline{IRQ}$	\$FFF8 (Upper address), \$FFF9 (Lower address)

The  $\overline{IRQ}$  signal to the CPU is output from the MN1271.

The MN1271 receives interrupt requests and generates the  $\overline{IRQ}$  signal to the CPU as a logical sum of them.

**Interrupt requests**

a.  $\overline{KON}$  signal

Indicating that the keyboard interface has detected the ON key.

b.  $\overline{SYSINT}$  signal

Interrupt request signal reserved by the system, for future system extension.

c.  $\overline{USERINT}$  signal

Interrupt request signal controllable by users with extension units.

d. Interrupt request signal generated in the MN1271

- Timer interrupt request signal
- Serial interface interrupt request signal

The  $\overline{NMI}$  signal is connected to the KSTOP signal generated when the BREAK key is depressed.

## 9. Character Code

### 9.1. Display Code Table (Hexadecimal Value)

Upper Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		~ (sp)	0	@	P	`	p								○	◻
1		÷	!	l	A	Q	a	q	♠						◻	◻
2		α	▼	2	B	R	b	r	♥						◻	◻
3		β	#	3	C	S	c	s	♦						◻	◻
4		γ	\$	4	D	T	d	t	♣						◻	◻
5		Σ	%	5	E	U	e	u	★						◻	◻
6		θ	&	6	F	V	f	v	←						◻	◻
7		◻	▼	7	G	W	g	w	↓						◻	◻
8		◻	(	8	H	X	h	x	↑						◻	◻
9		◻	)	9	I	Y	i	y	→						◻	◻
A		◻	*	:	J	Z	j	z	人						◻	◻
B		♪	+	;	K	[	k	{	☹						◻	◻
C		⊙	,	<	L	¥	l		◻	◻					◻	●
D		〒	-	=	M	]	m	}	◻	◻					◻	◻
E	☎	◎	·	>	N	^	n	—	◻	◻					◻	◻
F	π		/	?	O	_	o	(DEL)	◻	◻					◻	◻

Note:

1. SP means Space.
2. Display and Characters respectively indicated by shaded areas are actually assigned to Japanese Characters.

### 9.2. Character (ASCII) Code Table (Hexadecimal Value)

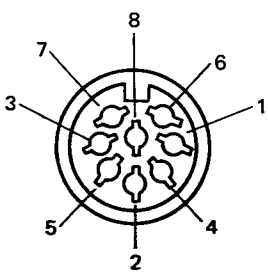
Upper Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NULL		(sp)	0	@	P	`	p	Graph on						○	◻
1			!	l	A	Q	a	q	♠						◻	◻
2			▼	2	B	R	b	r	♥						◻	◻
3	BRE AK	INS	#	3	C	S	c	s	♦						◻	◻
4		Graph off	\$	4	D	T	d	t	♣						◻	◻
5			%	5	E	U	e	u	★						◻	◻
6		HCO PY	&	6	F	V	f	v	←						◻	◻
7			▼	7	G	W	g	w	↓						◻	◻
8	RUB OUT	CAN SEL	(	8	H	X	h	x	↑						◻	◻
9			)	9	I	Y	i	y	→						◻	◻
A		LINS	*	:	J	Z	j	z	人						◻	◻
B	HOME		+	;	K	[	k	{	☹						◻	◻
C	CLS	→	,	<	L	¥	l		◻	◻					◻	●
D	RET URN	←	-	=	M	]	m	}	◻	◻					◻	◻
E		↑	·	>	N	^	n	—	◻	◻					◻	◻
F		↓	/	?	O	_	o		◻	◻					◻	◻

Note:

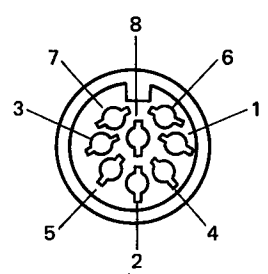
1. SP means Space.
2. Display and Characters respectively indicated by shaded areas are actually assigned to Japanese Characters.

## 10. Connector Pin Identification

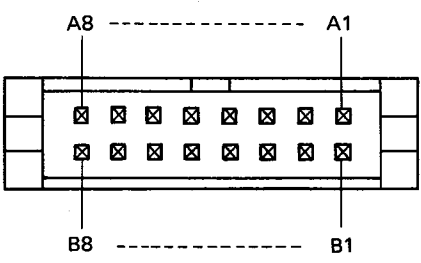
### 10.1. Display Connector

Pin No.	Signal	I/O	Pin Connection
1	NC		
2	GND		
3	Video	output	
4	H-SYNC	output	
5	V-SYNC	output	
6	R	output	
7	G	output	
8	B	output	

### 10.2. Tape Recorder Connector

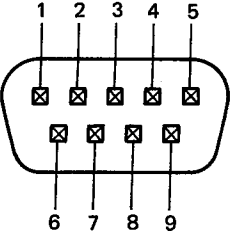
Pin No.	Signal	I/O	Pin Connection
1	GND		
2	GND		
3	GND		
4	REC	output	
5	MON	input	
6	REM1		
7	REM2		
8	GND		

### 10.3. Printer Connector

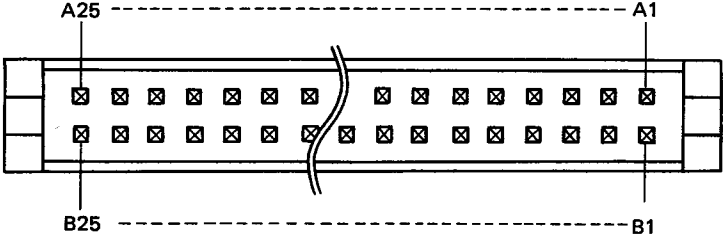
Pin No.	Signal	I/O	Pin Connection
A1	PDATA0	output	
A2	PDATA1	output	
A3	PDATA2	output	
A4	PDATA3	output	
A5	PDATA4	output	
A6	PDATA5	output	
A7	PDATA6	output	
A8	PDATA7	output	
B1	STROBE	output	
B2	GND		
B3	INITIAL	output	
B4	GND		
B5	BUSY	input	
B6	GND		
B7	PSEL	input	
B8	GND		



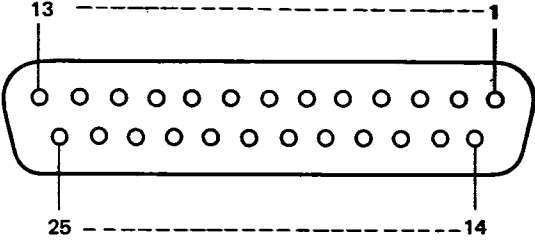
**10.4 Joystick Connector**

Pin No.	Signal (Joystick 1, Joystick 2)		I/O	Pin Connection
1	KIN0	KIN0	input	
2	KIN1	KIN1	input	
3	KIN2	KIN2	input	
4	KIN3	KIN3	input	
5	+5 V	+5 V		
6	KIN4	KIN4	input	
7	KIN5	KIN5	input	
8	KST8	KST9	output	
9	GND	GND		

**10.5. External Bus Connector**

Pin Connection					
					
Pin No.	Signal	I/O	Pin No.	Signal	I/O
A1	GND	input/ output	B1	GND	input/ output
A2	DB0	input/ output	B2	DB1	input/ output
A3	DB2	input/ output	B3	DB3	input/ output
A4	DB4	input/ output	B4	DB5	input/ output
A5	DB6	input/ output	B5	DB7	input/ output
A6	A0	output	B6	A1	output
A7	A2	output	B7	A3	output
A8	A4	output	B8	A5	output
A9	A6	output	B9	A7	output
A10	A8	output	B10	A9	output
A11	A10	output	B11	A11	output
A12	A12	output	B12	A13	output
A13	A14	output	B13	A15	output
A14	DRAMSEL	input	B14	$\overline{E\theta_2}$	output
A15	DRAM0 IN	output	B15	DRAM1 IN	output
A16	DRAM0 OUT	input	B16	DRAM1 OUT	input
A17	ADSEL	output	B17	TCAS	output
A18	$\overline{RAS}$	output	B18	$\overline{KILL}$	input
A19	+5 V		B19	+5 V	
A20	GND		B20	GND	
A21	$\overline{ER/W}$	output	B21	BA	output
A22	$\overline{HALT}$	input	B22	$\overline{VMA}$	output
A23	$\overline{SYSINT}$	input	B23	$\overline{USRINT}$	input
A24	$\overline{E\theta_2S}$	output	B24	$\overline{ERESET}$	output
A25	GND		B25	GND	

**10.6. RS-232C Connector (Optional)**

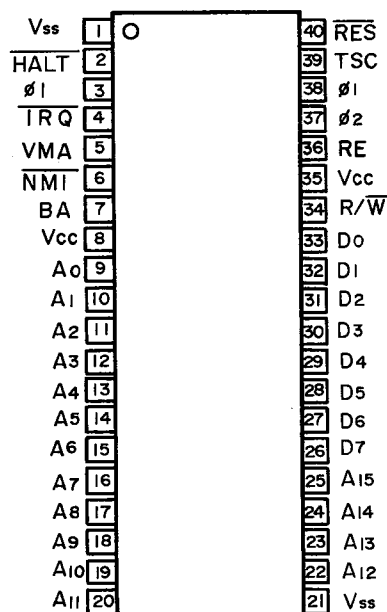
Pin No.	Signal	I/O	Pin Connection
2	SD	output	
3	RD	input	
4	RS	output	
5	CS	input	
6	DR	input	
7	SG		
8	CD	input	
20	ER	output	

Other Pins are NC.

## 1. LSI & IC Pin Configuration

### 11.1. MN1800A CPU

Pin Assignments



(Viewed from above)

(1) Ground (Vss) (pins 1, 21)

(2) HALT (pin 2)

When this line is "H" the CPU receives and executes instructions. When it goes "L" the CPU halts processing after completion of the current instruction.

(3) Phase 1 Clock (pin 3)

The system clock φ1 is input to this pin.

(4) Interrupt Request Line (IRQ) (pin 4)

When the interrupt mask is not set and the PIA (or another external device)  $\overline{\text{IRQ}}$  line goes "L", the CPU generates interrupt after completing the current instruction.

(5) Valid Memory Address (VMA) (pin 5)

This line is connected to all devices connected to the address lines from the CPU. When it is "H" it indicates that a valid address is on the address bus.

(6) Nonmaskable Interrupt ( $\overline{\text{NMI}}$ ) (pin 6)

This interrupt is the same as  $\overline{\text{IRQ}}$  except that it cannot be masked with the "I" bit. As with  $\overline{\text{IRQ}}$ , the current instruction is completed before the  $\overline{\text{NMI}}$  routine is executed.

(7) Bus Available (BA) (pin 7)

This line is normally "L" to indicate that the address and data buses are under the control of the CPU. When it goes "H" the address and data buses may be used by devices other than the CPU.

(8) +5 V Power (Vcc) (pin 8, 35)

(9) Address Lines (A0~A15) (pins 9~20, 22~25)

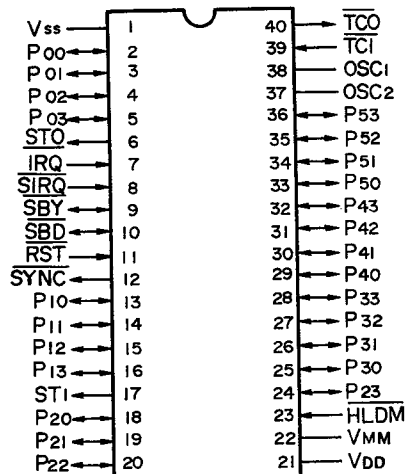
These 16 output lines are used to address devices other than the CPU.

(10) Data Lines (D0~D7) (pins 26~33)

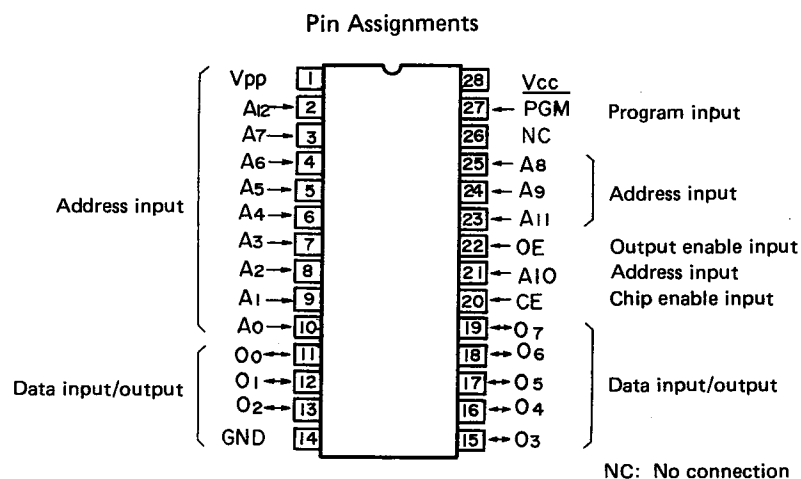
These 8 bi-directional lines are used to transfer data between the CPU and peripheral devices.

- (11) **Read/Write Control (R/W)**  
This signal is active low. When it is "L", it indicates to all external devices that the CPU is in a read or write operation.
- (12) **RAM Enable (RAME)**  
When this signal is "L", it enables the RAM.
- (13) **Phase 2 Clock (P2C)**  
The signal is active low and is used for the phase 2 clock.
- (14) **Three-Stage Control (TSC) (pin 39)**  
When this signal is "H" all address lines and the R/W line assume the high impedance condition and VMA and BA go "L".
- (15) **Reset (RES) (pin 40)**  
This input signal is used to start the CPU from the power down condition. The RES input must be maintained at "L" for a minimum of 8 clock cycles after voltage reaches 4.75 V. During this interval the address bus outputs the address \$FFFE.

## 11.2. MN1544CJR Sub CPU

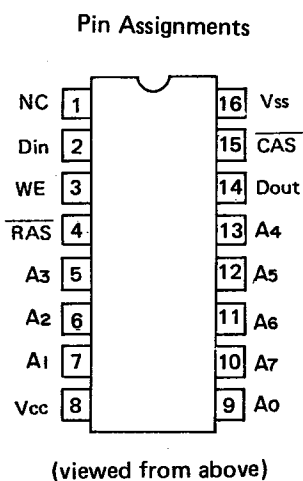


VDD	Power supply (+5 V)
VMM	RAM power supply
Vss	Power supply (GND)
OSC1, OSC2	Clock generator terminals (OSC1 is for external clock input)
SYNC	Internal cycle synchronizing signal output
IRQ	Program control interrupt input
SIRQ	Maximum priority interrupt input
SBD	Serial input
SBY	Serial I/O clock input
TCI	Timer/counter input
TCO	Timer/counter output
HLD	RAM power supply maintenance specification
RST	Reset signal input
P00~P53	Parallel I/O port
ST0, ST1	Strobe output for I/O ports P0 and P1

**11.3. MN4864CA2 (ROM 0), MN4864CB2 (ROM 1)**

(viewed from above)

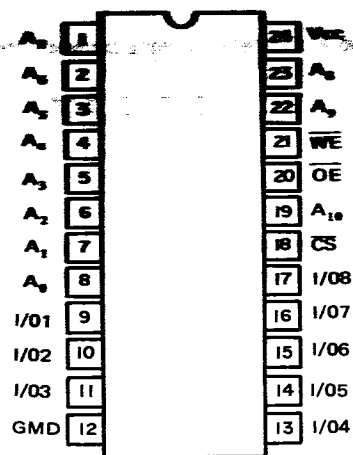
A0~A12 Address input  
 O0~O7 Data input/output  
 PGM Program input  
 OE Output enable  
 CE Chip enable input

**11.4. HM4864P3 RAM**

A0~A7	Address input
CAS	Column address strobe
Din	Data input
Dout	Data output
RAS	Row address strobe
WE	Read/Write input
Vcc	Power supply (+5 V)
Vss	GND

## 11.5. HM6116P3 RAM

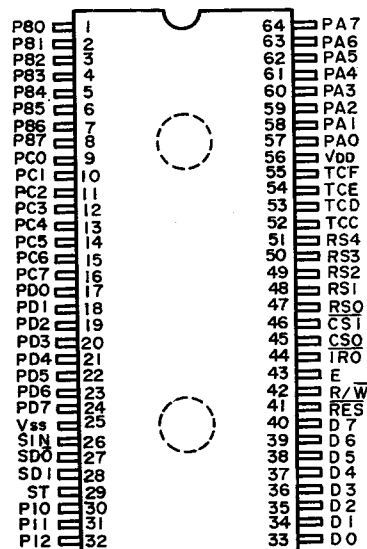
Pin Assignments



(viewed from above)

A0~A10	Address input
I/O1~I/O7	Data input/output
WE	Read/Write input
OE	Output enable
CS	Chip select input

## 11.6. MN1271 PIA



### (1) 8-bit Parallel Ports (PA0~PA7, PB0~PB7, PC0~PC7, PD0~PD7)

The PIA supports four 8-bit parallel ports (PA, PB, PC, PD), each port having an 8-bit data register and direction register to permit single bit input/output. The direction register is set to input with "0" and output with "1".

### (2) 3-bit Parallel Port (PI0~PI2)

The 3-bit parallel port supports a mode register, a data register, and an edge detection register for level input edge detection (rising edge, falling edge), level output, and pulse output.

### (3) Serial Port (SD0, SD1, ST)

This port is used for transmission and reception of serial data, data being transmitted from SD0 and received at SD1. The timing clock signal required for transmission/reception is supplied to ST.

**(4) Sine Wave Generation (SIN)**

The 3-bit precision stepped wave generated with output under the control of the timer/counter is output from SIN.

**(5) Data Bus (D0~D7)**

The bi-directional data bus is used for transfer of data between the CPU and the MN1271.

**(6) Timer/Counter Input/Output (TCC, TCD, TCE, TCF)**

TCC, TCD: 8-bit timer/counters

TCE, TCF: 16-bit timer/counters

Frequency divided waveforms are output in the timer mode, and input pulses are counted in the event count mode. E and F support a pulse width measurement function as well.

**(7) Register Select (RS0~RS4)**

Five signal input pins (5 bits) for register selection.

**(8) Chip Select (CS0,  $\overline{\text{CS1}}$ )**

Chip select signal input pins, the chip is selected when CS0 is "H" and CS1 and " $\overline{\text{L}}$ ".

**(9) Interrupt Request ( $\overline{\text{IRQ}}$ )**

Interrupt requests for registers within the PIA. OR is taken within the chip and the IRQ signal output from this pin. The  $\overline{\text{IRQ}}$  signal is active low, and may be connected with other interrupt signals in a wired OR configuration.

**(10) Enable (E)**

The MC6800  $\phi 2$  clock is normally input to this pin.

**(11) Reset ( $\overline{\text{RES}}$ )**

A " $\overline{\text{L}}$ " signal is input to this pin to apply system reset to the chip. System reset is cleared by writing "0" into the MSB of the edge detection register.

**(12) Read/Write (R/ $\overline{\text{W}}$ )**

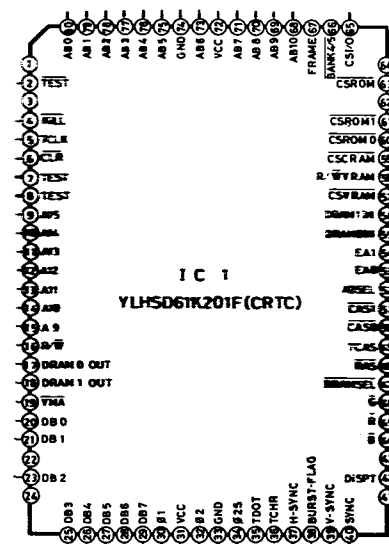
The CPU reads data when this signal is "H" and write data when it is " $\overline{\text{L}}$ ".

**(13) Vss**

Normally connected to 0 V or GND.

**(14) VDD**

Normally connected to +5 V.



RAS	RAS timing signal
TCAS	CAS timing signal
	To be used after ANDing with chip select signals
ADSEL	Address select signal
	Timing for switching addresses for rows and columns
DRAM0 IN	Input data signal to DRAM
DRAM1 IN	"
DRAM0 OUT	Output data signal from DRAM
DRAM1 OUT	"
EA0, EA1	External address signal
R/W VRAM	Read/write signals to VRAM and CRAM
<u>KILL</u>	ROM0 kill signal (IC5) If this terminal is set at low level, the system ROM becomes invalid. (IC5)
<u>DRAMSEL</u>	RAM select signal (negative) If this terminal is set at low level, the control signals are output when a 64K dynamic RAM is used. The chip select signal is input to the terminal.

(EXTERNAL)

**Device-select signals are generated to select devices allocated on the memory map.**

Signal Name	Application
<u>CAS0</u>	for DRAM (IC8, IC10)
<u>CAS1</u>	for DRAM (IC9, IC11)
<u>CSV RAM</u>	for VRAM (IC7)
<u>CSC RAM</u>	for CRAM (IC6)
<u>CS I/O</u>	for DIA (IC17)
<u>CSROM0</u>	for ROM (IC5)
<u>CSROM1</u>	for ROM (IC4)



**(3) System Clock Generation**

TCLK is the crystal oscillator frequency with a middle frequency of 14.31818 MHz (four times higher than the  $\phi 1$  and  $\phi 2$  are the two-phase clocks required by the CPU.

$\phi 2S$  is a clock required by peripheral LSI.

**(4) CRT Control Signals Generation**

a. For RGB Signal Processor

$\overline{R}$	Color (Red) Signal
$\overline{G}$	Color (Green) Signal
$\overline{B}$	Color (Blue) Signal
H-SYNC	Horizontal Synchronizing Signal
V-SYNC	Vertical Synchronizing Signal

b. For Composite Signal Processor

$\overline{R}$	Color (Red) Signal
$\overline{G}$	Color (Green) Signal
$\overline{B}$	Color (Blue) Signal
SYNC	Synchronizing Signal
BURST FLAG	Burst Signal (3.579545 MHz)

**(5) Address Bus/Data Bus**

A9~A15	Address bus signals from CPU
AB0~AB10	Address bus signals to VRAM and CRAM
DB0~DB7	Data bus signals from CPU, VRAM and CRAM

**(6) Control Signal from CPU**

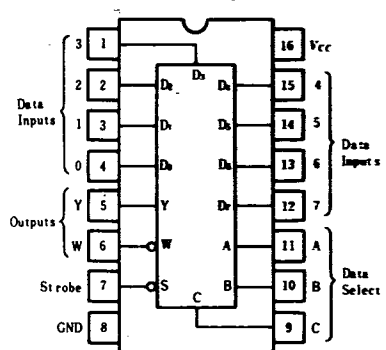
$R/\overline{W}$	Read/Write Control Signal
VMA	Valid Memory Address Signal

**(7) Refresh Address Generation**

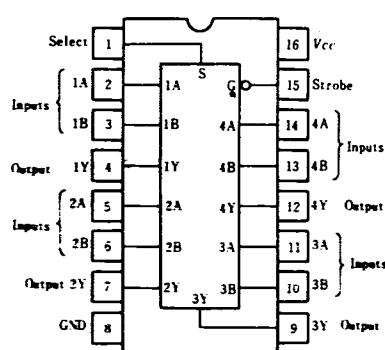
AB0 to AB6 are required for the  $\overline{RAS}$ -only refresh, but these signals are not available. It is, therefore, preferable to use a RAM with the refresh function built-in.

## 11.8. TTL ICs

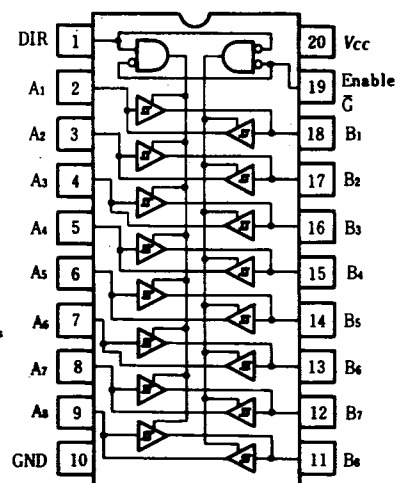
LS151



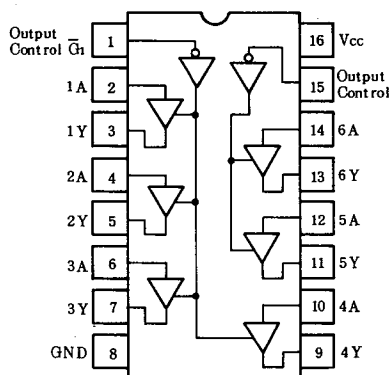
LS157



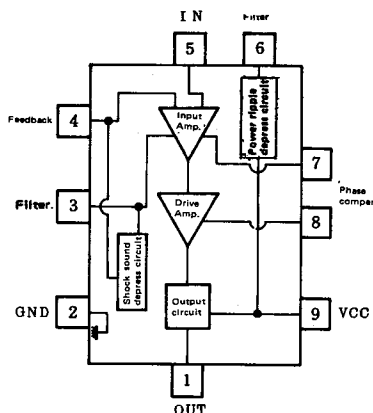
LS 245



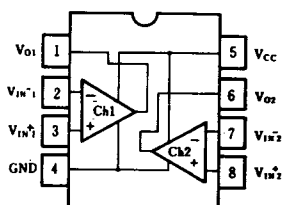
LS367



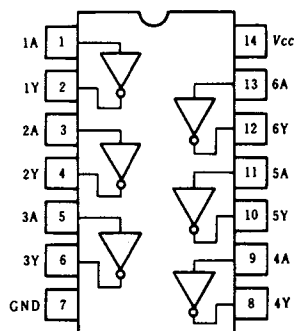
7117



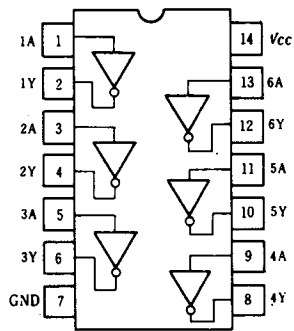
AN6914



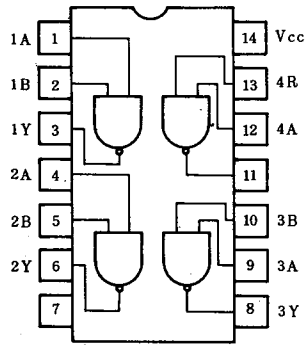
7416



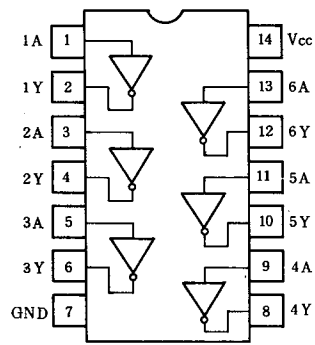
7404



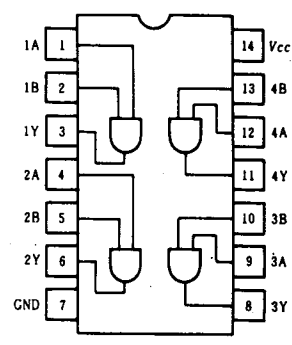
LS00



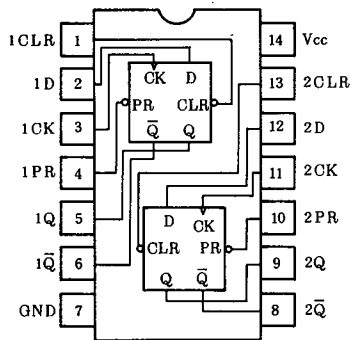
LS04  
LS05



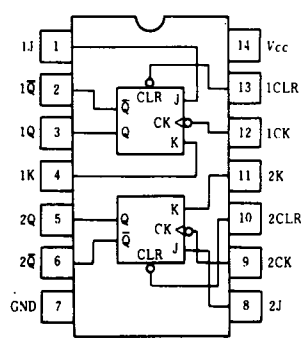
LS08



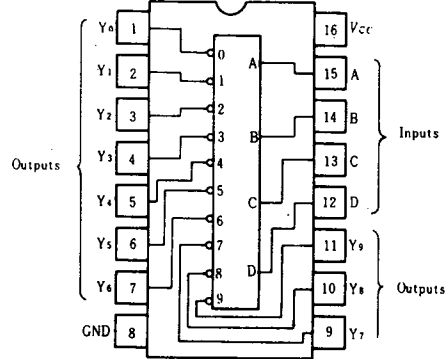
LS74



LS107



LS145



## 12. Disassembly

Disassemble JR-200U in the following manner with care not to damage the cabinet.

- 1) Place the JR-200U up side down.
- 2) Remove 6 screws from the lower case.
- 3) Remove the upper case from the lower case while pushing 2 points as indicated.  
Be careful not to damage the multi lead connecting the keyboard and the main P.C.B.
- 4) Pull the LED out of the upper case.
- 5) Remove the speaker from the upper case after removing 2 screws.
- 6) Clear six spurs, and remove the keyboard panel from the upper case.
- 7) Remove nine screws fastening the shield case (B) and remove the shield case B.
- 8) Remove the connector from the power transformer to the main P.C.B., four screws fastening the power transformer and two screws fastening the noise filter, and remove the power supply assembly.



Fig. 1

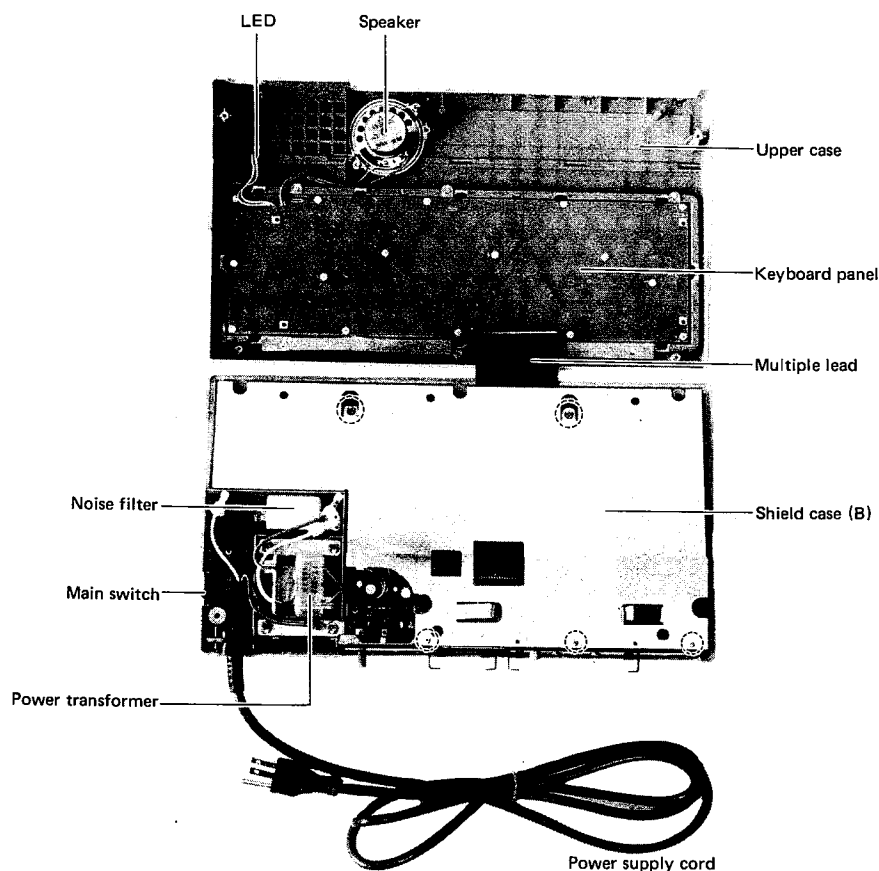


Fig. 2

### 13. Exploded View

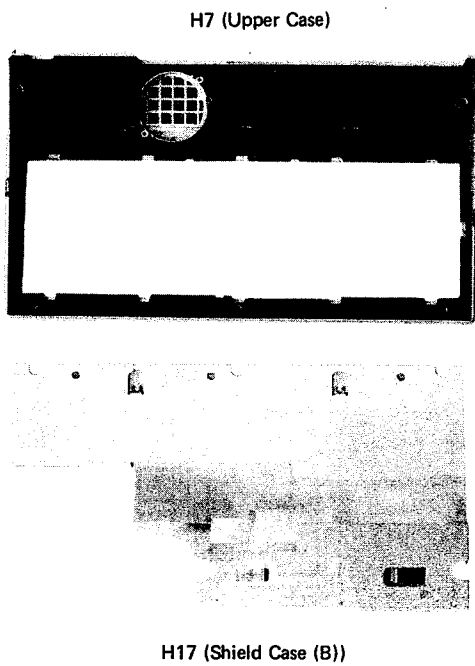


Fig. 1

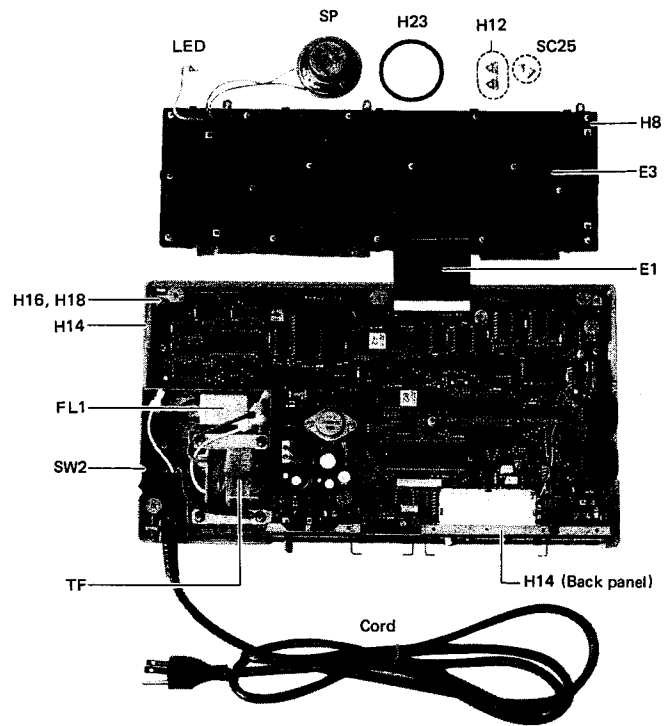


Fig. 2

#### ● Accessories

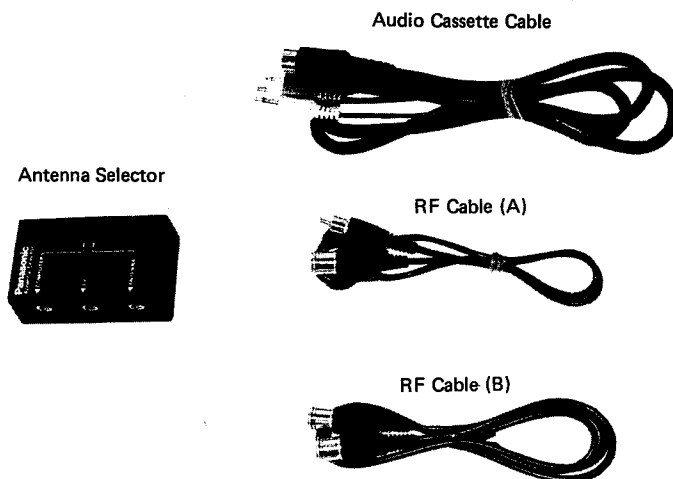
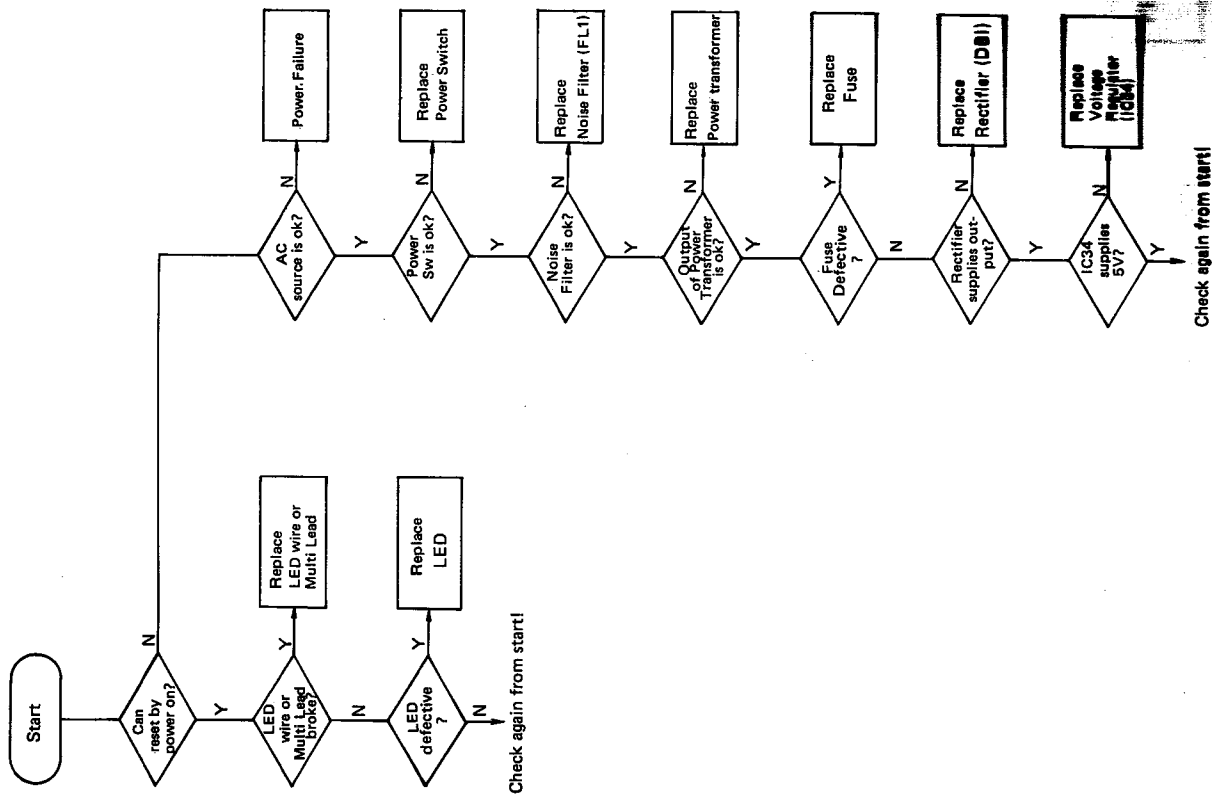


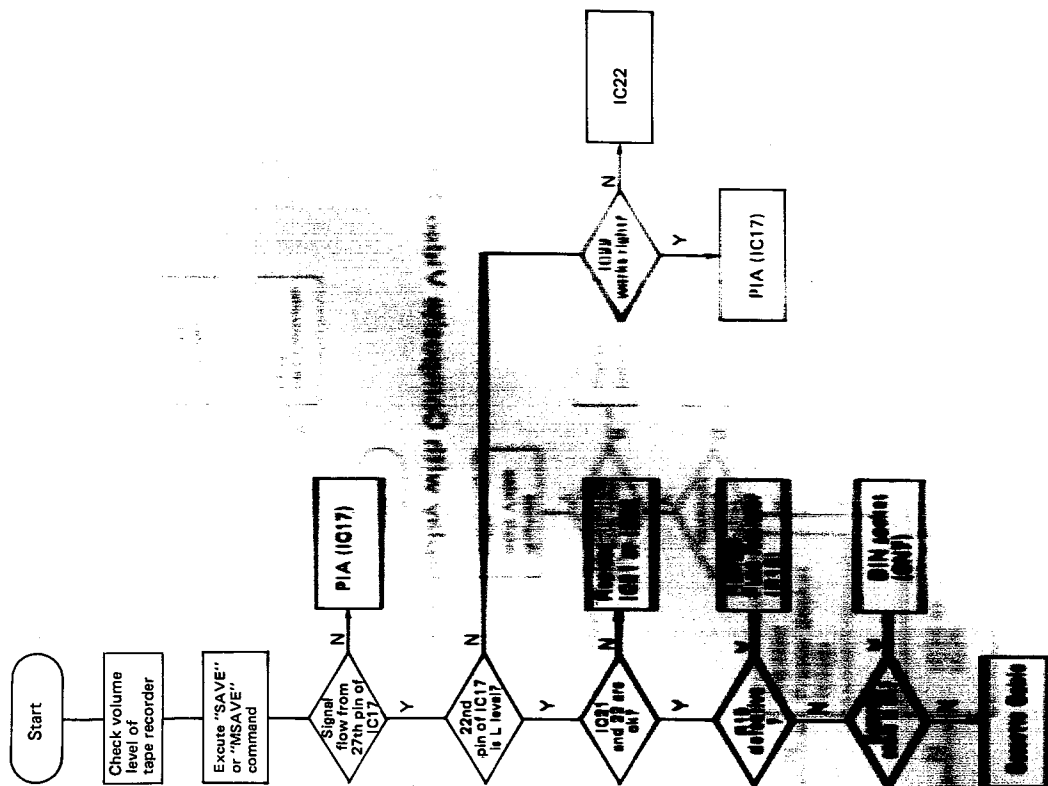
Fig. 3

## 14. Troubleshooting

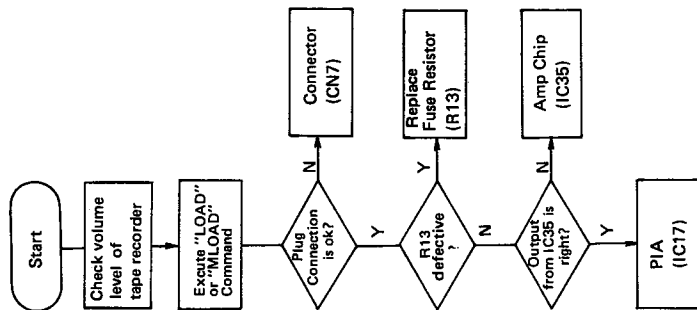
### (1) Power Indicator Does Not Light Up



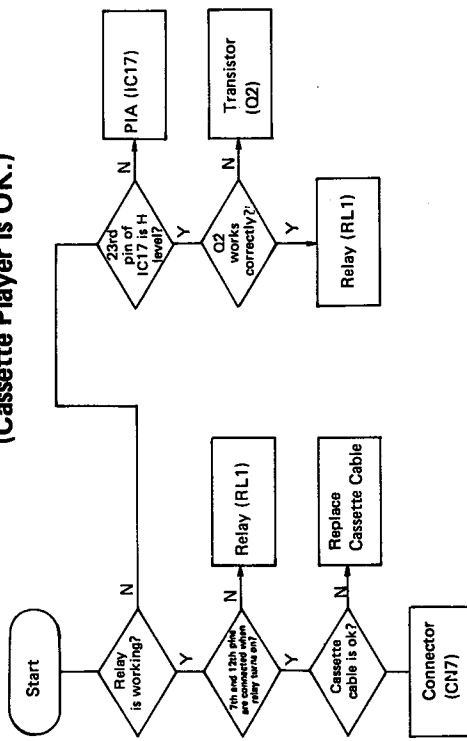
### (2) Can't SAVE or MSAVE (Cassette Player is OK.)



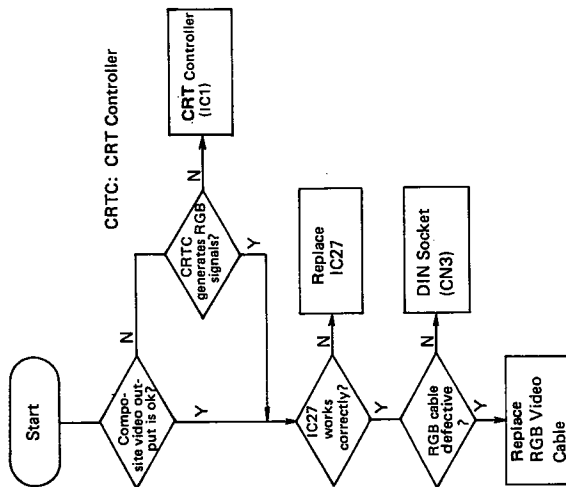
(3) Can't LOAD or MLOAD (Cassette Player is OK.)



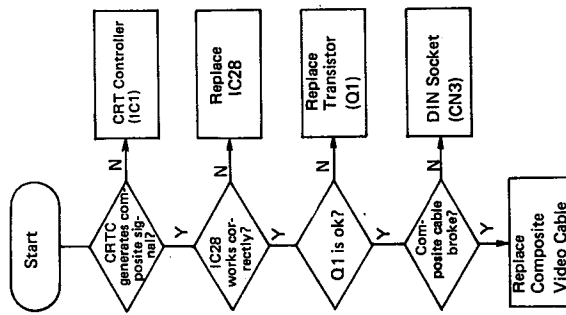
(4) Remote Control of Cassette Player Won't Work (Cassette Player is OK.)



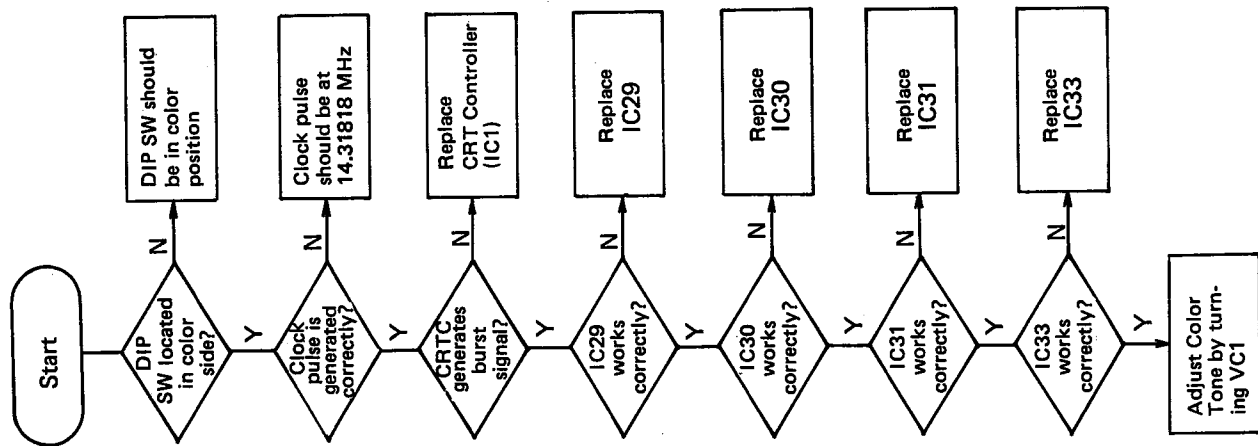
(5) No Display with RGB Video Terminal (RGB Monitor is OK.)



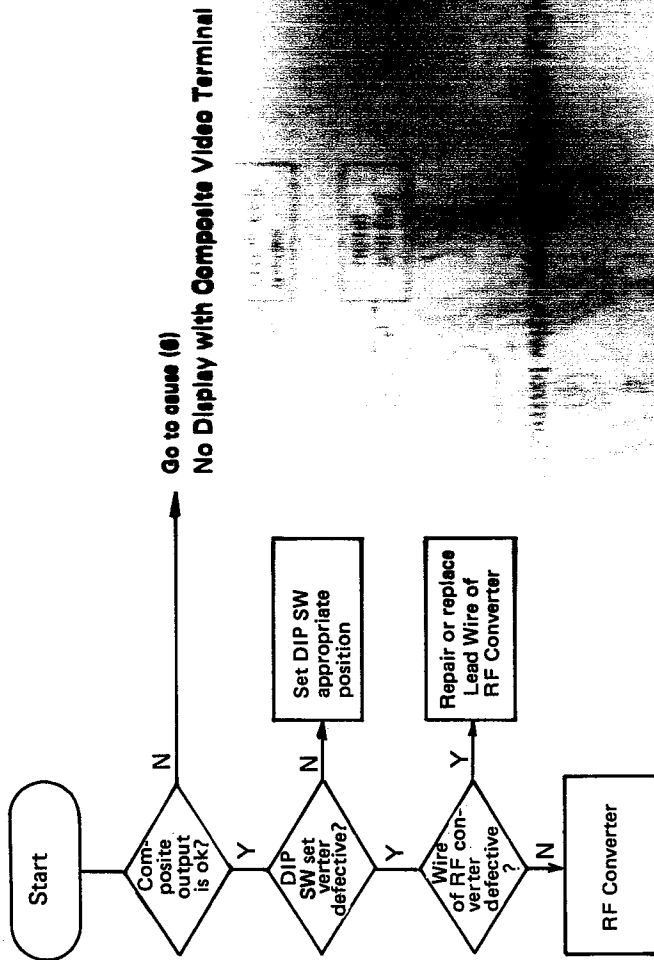
(6) No Display with Composite Video Terminal (TV is OK.)



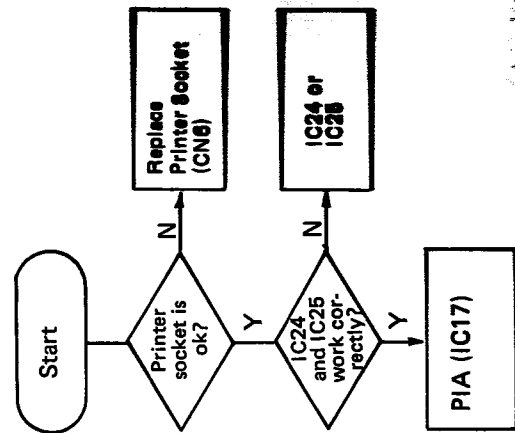
**(7) No-Color Display with Composite Video Terminal  
(TV is OK)**



**(8) No Display with RF Terminal (TV is OK.)**

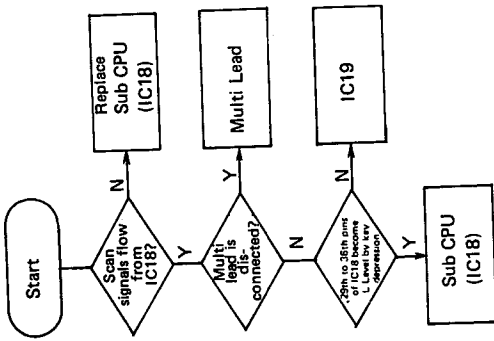


**(9) Printer Won't Print (Printer is OK.)**

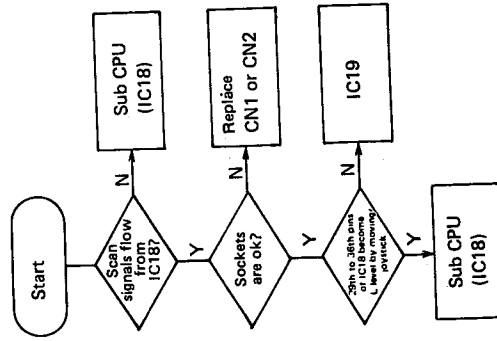




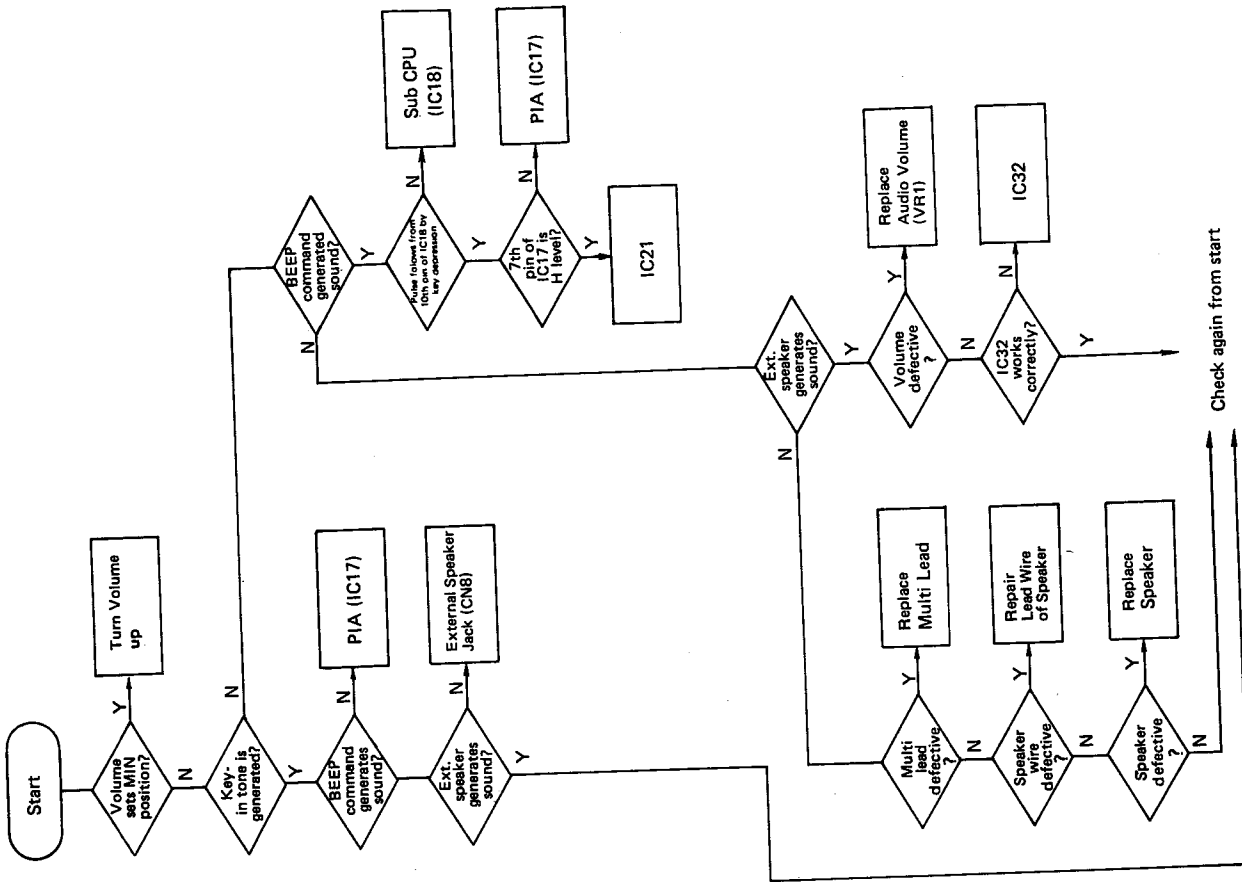
# (11) Key Won't Make

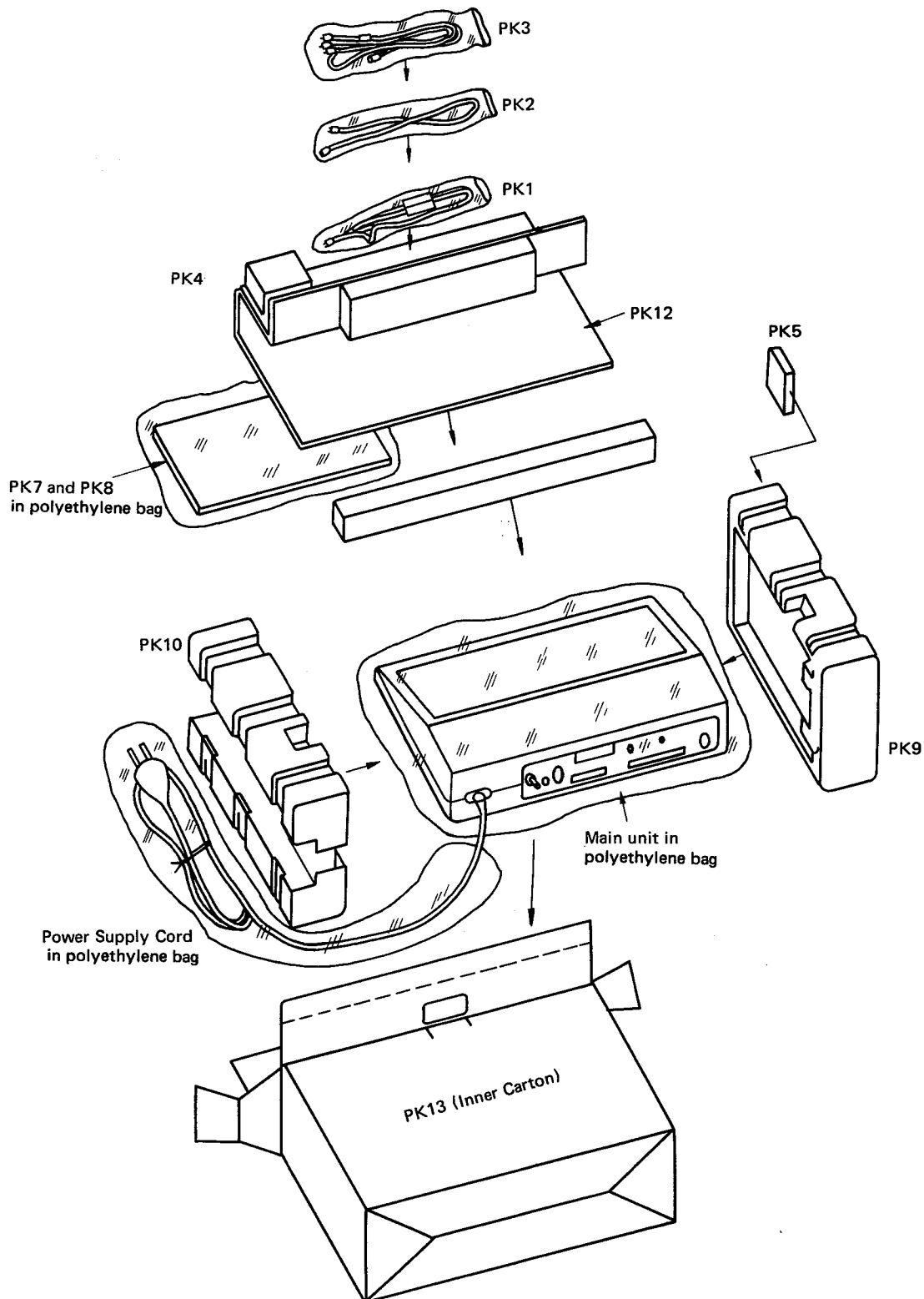


# (12) Can't Control with Joystick (Joystick is OK)



# (10) Sound is Not Generated






# 16. Replacement Parts List

Model: JR-200U



**Note:**  
 • When ordering replacement parts, indicate Part No. and Name of Part.  
 •  Indicates that only parts specified by the manufactures be used for replacement in critical circuits.

Ref. No.	Part No.	Part Name & Descriptions	Pcs/Set	Remarks
<b>MAIN CIRCUIT BOARD &amp; KEYBOARD</b>				
IC2	MN1800A	Main CPU	1	
IC18	MN1544CJR	Keyboard Controller (Sub CPU)	1	
IC4	MN4864CA2	ROM (8KB)	1	
IC5	MN4864CB2	ROM (8KB)	1	
IC8-11	YLHSHM4864P3	Dynamic RAM (64 K bits)	4	
IC6, 7	YLHSHM6116P3	Static RAM (2KB)	2	
IC17	MN1271	I/O Controller (PIA)	1	
IC1C	YLHSD61K201F	CRT Controller	1	
IC23	DN74LS00	TTL IC	1	
IC22, 28, 24-26	DN74LS04	TTL IC	5	
IC20	DN74LS05	TTL IC	1	
IC21, 29	DN74LS08	TTL IC	2	
IC30	DN74LS74A	TTL IC	1	
IC31	DN74LS107	TTL IC	1	
IC19	DN74LS145	TTL IC	1	
IC33	YLHSH74LS151	TTL IC	2	
IC12, 13	DN74LS157	TTL IC	1	
IC3	YLHSH74LS245	TTL IC	2	
IC14, 15	DN74LS367A	TTL IC	1	
IC16	YLHSHD7404P	TTL IC	1	
IC27	YLHSHD7416P	TTL IC	1	
IC32	AN7117	Power Amplifier	1	
IC35	AN6914	Comparator	1	
IC34	YLH818053B	IC (Voltage Regulator)	1	
Q1, 2	2SD636	Transistor	2	
D1-3	YLUDTS2473T	Diode	3	
D4	YLUD10E1T	Diode	1	
X1	EYXBD146S20	Crystal (14.31818 MHz)	1	
RL1	AG2019	DS Relay	1	
E1	YLWJL222X70	Multi Lead	1	
SW1	YLSJS874703	Dip Switch 3p	1	
R37	ERD25TJ750T	Resistor	1	1/4 W 75 ohm
R23, 24	ERD25TJ101T	Resistor	2	1/4 W 100 ohm
R7, 22	ERD25TJ151T	Resistor	2	1/4 W 150 ohm
R38, 43, 44, 47	ERD25TJ331T	Resistor	4	1/4 W 330 ohm
R32	ERD25TJ471T	Resistor	1	1/4 W 470 ohm
R18, 36	ERD25TJ561T	Resistor	2	1/4 W 560 ohm
R35	ERD25TJ681T	Resistor	1	1/4 W 680 ohm
R17, 31	ERD25TJ102T	Resistor	2	1/4 W 1 k
R27, 30	ERD25TJ122T	Resistor	2	1/4 W 1.2 k
R4	ERD25TJ152T	Resistor	1	1/4 W 1.5 k
R5, 33, 38	ERD25TJ222T	Resistor	3	1/4 W 2.2 k
R28	ERD25TJ242T	Resistor	1	1/4 W 2.4 k

Brought to you by Vintage Volts - <http://www.vintagevolts.com>

Ref. No.	Part No.	Part Name & Descriptions	Pcs/Set	Remarks
R16, 29, 19-21, 40	ERD25TJ472T	Resistor	6	1/4 W 4.7 k
R14	ERD25TJ562T	Resistor	1	1/4 W 5.6 k
R1-3, 6, 9-12, 15, 24-26	ERD25TJ103T	Resistor	11	1/4 W 10 k
R8	ERD25TJ473T	Resistor	1	1/4 W 47 k
R39	ERD25TJ224T	Resistor	1	1/4 W 220 k
R15	ERD2FCG680P	Fuse Resistor	1	1/4 W 68 ohm
R13	ERQ12HJ151P	Fuse Resistor	1	1/2 W 150 ohm
VR1	EVJEAAE03B14	Variable Resistor	1	10 k
RA1	EXBP85103K	Resistor Array	1	10 k X 5
RA2	EXBP85331K	Resistor Array	1	330 X 5
C31	ECEA1HS2R2	Electrolytic Capacitor	1	50 V 2.2
C38	ECEA1HS471	Electrolytic Capacitor	1	50 V 470
C1, 35	ECEA1AS330	Electrolytic Capacitor	2	10 V 33
C32, 34, 41	ECEA1AS101	Electrolytic Capacitor	3	10 V 100
C33	ECEA1AS331	Electrolytic Capacitor	1	10 V 330
C36	ECEA1AS471	Electrolytic Capacitor	1	10 V 470
C37	ECEA1AS102	Electrolytic Capacitor	1	10 V 1000
C27	YLCQMS05103K	Polyester Capacitor	1	50 V 0.01 $\mu$
C17	ECBT1H270JC	Ceramic Capacitor	1	50 V 27 P
C22, 33	ECBT1H390K	Ceramic Capacitor	2	50 V 39 P
C54-56	ECBT1H101KB	Ceramic Capacitor	1	50 V 100 P
C11	ECBT1H151KB	Ceramic Capacitor	1	50 V 150 P
C44	ECBT1H391KB	Ceramic Capacitor	1	50 V 390 P
C16	ECCW1H221JC	Ceramic Capacitor	1	50 V 220 P
C18	ECCW1H331JL	Ceramic Capacitor	1	50 V 330 P
C28, 43	ECBT1H561KB	Ceramic Capacitor	2	50 V 560 P
C45-52	ECKF1H331KB	Ceramic Capacitor	8	50 V 1000 P
C39	ECKW1H103KB	Ceramic Capacitor	1	50 V 0.01 $\mu$
C2-10, 20, 23-26, 27, 28	ECBT1C223ND	Ceramic Capacitor	22	16 V 22000 P
C57	ECBT1H221KB	Ceramic Capacitor	1	50V 220 P
VC1	ECV12W40X53T	Variable Capacitor	1	40 P
VC2	ECV12W20X53T	Variable Capacitor	1	20 P
RFC	YLBX45000600	RF Converter (American CH.)	1	
CN8	YLOJSQ3096	Pin Jack (for Ext. Speaker)	1	
CN5	YLOP5001120N	Connector 50 P (for Expansion)	1	
CN6	YLOP1601120N	Connector 16 P (for Printer)	1	
CN1, 2	YLOQA2074561	Connector 9 P (for Joysticks)	2	
CN3, 7	YLORTCS4480	Connector 8 P (DIN Jack)	2	
CN9	YLOPWP3002	Connector (F) 2 P (Power Supply)	1	
CN9	YLOPWA5002	Connector (M) 2 P (Power Supply)	1	
CN9	YLOPWT0502	Connector Terminal (for above)	2	
CN10	EMCS1252M	Connector 12 P (for RS232C Card)	1	
DB1	YLUDS2VB10	Rectifier	1	
FL2	YLPFNDSS310	Noise Filter	1	
FL3	YLPFNXMM9V	Low Pass Filter	1	
FL4-7	YLPFNDSB271M	EMI Filter	4	
L1, 2	ELQS470KB	Coil	2	
L3	YLPCSR02025	Coil	1	
L10	YLPCLF9H102J	Coil	1	
L4-9	YLPCEMCB3	Coil	6	

Ref. No.	Part No.	Part Name & Descriptions	Pcs/Set	Remarks
PK5	YLVTR0007400	Demonstration Cassette Tape	1	
PK6	TJB-525000	Antenna Plug	(1)	
PK7	YLMZH0009700	Warranty Card	1	
PK8	YLEX76003600	Operating Instructions	1	
PK9	YLMZC0116500	Inner Styrol (R)	1	
PK10	YLMZC0116600	Inner Styrol (L)	1	
PK11	YLMZC0119300	Styrol Pad	1	
PK12	YLMZC0116700	Inner Pad	1	
PK13	YLMZC0121600	Inner Carton	1	

Ref. No.	Part No.	Part Name & Descriptions	Pcs/Set	Remarks
E2	YLP45B00100	Shield Plate Ass'y (including feed through capacitors)	1	
E3	YLP4RK0010800	Keyboard P.W.B.	1	
LED	LN819RP	LED	1	
SP	EAS5PT3S	Speaker	1	
<b>POWER SUPPLY ASS'Y</b>				
TF	YLP4TIT322	Power Transformer (120 V)	1	
FUSE	YLP4TIT322	Fuse 125 V 1.0 A	1	
PS1	YLP4HSN5053	Fuse Holder	2	
PS2	YLP4TGT0003300	Solderless Terminal	1	
COR	YLP4BWR5956	Power Supply Cord	1	
SW2	YLP4SVWK2A44	Power Switch	1	
FL1	YLP4FNMCMC2020	Noise Filter	1	

**HOUSING**

H1	YLLIA0077500	Supply Panel	1	
H2	YLLIG0010700	FCC Label	1	
H3	YLLIG0010900	Caution Label	1	
H4	YLMC45B34200	Lower Case Ass'y	1	
H5	YLLIH0017900	Switch Label	1	
H6	YLLIH0018000	Joy Stick Label	1	
H7	YLMC45A50300	Upper Case Ass'y	1	
H8	YLMCG0056600	Keyboard Panel	1	
H9	YLOTFO022500	Contact Rubber (1)	1	
H10	YLOTFO022600	Contact Rubber (2)	1	
H11	YLOTFO022700	Contact Rubber (3)	1	
H12	YLOTFO020500	Contact Rubber (4)	1	
H13	YLP4SB0000400	Shield Sheet (for keyboard panel)	1	
H14	YLMCG0056700	Back Panel	1	
H15	YLMIM0008200	Masking Plate	1	
H16	YLMCC0005700	Shield Case (A) (lower)	1	
H17	YLMCC0005800	Shield Case (B) (upper)	1	
H18	YLMCK0011000	Shield Case Sheet (lower)	1	
H19	YLMCM00035100	Connector Cover	2	
H20	YLMUB00002700	Connector Earth Plate	2	
H21	YLMUB00001900	Hold Plate (for power transformer)	2	
H22	YVN101SA005A	Speaker Holder	2	
H23	YLLXB0006800	Speaker Pad (1)	1	
SC1	XTB3+10JFX	Screw (for Cabinet)	6	
SC2	XTB3+8JFX	Screw (for Main P.C.B. and Noise filter)	9	
SC3	XTB4+20JFX	Screw (for Power Transformer)	4	
SC4	XYN26+06FX	Screw (for Back Panel)	2	
SC5	XTB3+6JFX	Screw (for Speaker)	2	
SC6	YLLSA0003200	Screw (for Keyboard)	22	
SC7	XSB26+10FX	Screw (for Printer Connector & I/O Connector)	4	
SC8	XNG26H	Nut (for Printer Connector & I/O Connector)	4	
SC9	XTM26+6HFZ	Screw (for Masking Panel)	2	
SC10	XYN26+C5FN	Screw (for Shield Case)	3	
SC11	XSB+3FZ	Screw (for RF converter)	2	

**PACKING & ACCESSORIES**

PK1	YLBWR482800	RF Cable (A)	1	
PK2	YLBWR482800	RF Cable (B)	1	
PK3	YLBWCAST	Audio Cassette Cable	1	
PK4	YLSJR2000U	Antenna Selector	1	